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FINAL PROJECT REPORT

High-Performance Copper Plating on Silicon Photovoltaic Cells Using Low-Cost Printed Circuit Board Technology

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PREFACE

The California Energy Commission's (CEC) Energy Research and Development Division supports energy research and development programs to spur innovation in energy efficiency, renewable energy and advanced clean generation, energy-related environmental protection, energy transmission and distribution and transportation.

In 2012, the Electric Program Investment Charge (EPIC) was established by the California Public Utilities Commission to fund public investments in research to create and advance new energy solutions, foster regional innovation and bring ideas from the lab to the marketplace. The CEC and the state's three largest investor-owned utilities—Pacific Gas and Electric Company, San Diego Gas & Electric Company and Southern California Edison Company—were selected to administer the EPIC funds and advance novel technologies, tools, and strategies that provide benefits to their electric ratepayers.

The CEC is committed to ensuring public participation in its research and development programs that promote greater reliability, lower costs, and increase safety for the California electric ratepayer and include:

- Providing societal benefits.
- Reducing greenhouse gas emission in the electricity sector at the lowest possible cost.
- Supporting California's loading order to meet energy needs first with energy efficiency and demand response, next with renewable energy (distributed generation and utility scale), and finally with clean, conventional electricity supply.
- Supporting low-emission vehicles and transportation.
- Providing economic development.
- Using ratepayer funds efficiently.

High-Performance Copper Plating on Silicon Photovoltaic Cells Using Low-Cost Printed Circuit Board Technology is the final report for the High-Performance Copper-Plating on Silicon Photovoltaic Cells Using Low-Cost Printed Circuit Board Technology project (Contract Number EPC-16-035) conducted by Sunpreme Inc. The information from this project contributes to the Energy Research and Development Division's EPIC Program.

For more information about the Energy Research and Development Division, please visit the [CEC's research website](http://www.energy.ca.gov/research/) (www.energy.ca.gov/research/) or contact the CEC at 916-327-1551.

ABSTRACT

This project developed a cost-effective method to produce high performance heterojunction silicon photovoltaic cells with copper metallization by adapting a dry-resist lamination and high throughput laser scanning exposure toolset, originally developed for the printed circuit board industry, and a high throughput, high resolution plating tool, developed for the semiconductor industry. The innovative manufacturing approach can be transitioned from a pilot-scale (less than 50 wafers per hour and technology readiness level 5) to a high-volume manufacturing scale (technology readiness level 7), with capacity to produce 3300 wafers per hour.

The developed equipment and process will reduce module production costs by 75 percent to \$0.41 per watt at a 300 megawatt scale, while improving the cell efficiency by 2 percent and virtually enabling best-in-class cost and performance.

This manufacturing approach could be applied to virtually any type of silicon photovoltaic cell, enabling the broad-scale adoption of copper metallization at lower cost than silver paste.

The highest efficiency achieved in this project for photovoltaic cells with copper-patterning was 24 percent. Tools necessarily for a high-volume manufacturing process were developed and optimized. A detailed cost model confirms the potential of this innovative process to reduce costs by \$0.022 per watt compared to the silver-paste process.

Keywords: solar photovoltaic, copper metallization, cell efficiency, cost reduction.

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EXECUTIVE SUMMARY

Background

Today almost all solar photovoltaic manufacturing uses silver paste to print conducting wires on solar cells. Silver paste is expensive and low-resolution, which means the aspect ratio of metal patterning is only 1:2 (height: width) and less conductive compared to copper. Therefore, photovoltaic cells that use silver paste are less efficient than photovoltaic cells that use photolithographically patterned copper.

Silver-Paste Printing: Of the 75 gigawatts of solar manufacturing capacity worldwide, more than 98 percent use silver paste for metallization. At \$16 an ounce, silver represents more than 60 percent of the total wafer-to-cell manufacturing material cost. Silver prices in 2020 are down nearly 70 percent from their high of \$55 an ounce in 2011. A rebound in silver prices would severely affect panel manufacturing costs. Silver also has limitations on cell efficiency. Silver paste bulk resistivity is 10 ohms per centimeter, five times higher than copper, resulting in higher resistive losses. Printed silver-paste lines are wide and typically cause significant shading losses. Photo-patterned copper lines can be much thinner.

Copper Plating: Some photovoltaic manufacturers have proposed using copper plating as an alternative to silver paste to reduce metal costs, lower resistive losses, and deposit thinner lines, thereby reducing shading losses. However, only the San Jose-based solar panel manufacturer SunPower has commercialized copper in high volume manufacturing, using a complex process integration flow with high manufacturing costs. For copper metallization to be adopted broadly, a new approach is needed. This project developed copper-patterning technology on a laboratory scale that increased cell efficiencies by 1 to 2 percent (absolute efficiency) and reduced the cost of metallization by 50 percent relative to silver.

Project Purpose

This project developed a next-generation manufacturing toolset and process workflow for low-cost, high performance copper patterning on photovoltaic cells by adapting technologies from the highly cost-sensitive printed circuit board industry. Copper is an attractive alternative to silver paste because of its inherent conductive properties and lower material cost. However, today, only 2 percent of photovoltaic cells globally use copper plating, due to its complex and costly process, which uses spin-coating and photolithography. Conversely, the printed circuit board industry uses copper plating on a massive scale at a very low cost with alternative techniques that use dry photoresist films laminated onto the printed circuit board and pattern with standoff optics.

This project has demonstrated on a pilot scale how printed circuit board techniques can be adapted to photovoltaic manufacturing, while retaining the low-cost potential and accommodating the more fragile nature and higher resolution patterning requirements of photovoltaic wafers. When integrated in a high-volume manufacturing process, the tools and techniques developed under this project have the potential to increase the efficiency of commercially available heterojunction silicon photovoltaic cells by 10 percent (from 21.5 percent cell efficiency to greater than 23.5 percent cell efficiency) and reduce panel costs from \$0.61 per Watt peak to \$0.41 per Watt peak. The levelized cost of electricity without

investment tax credit would be \$0.036 per kilowatt-hour, exceeding the 2020 goals of SunShot Initiative of \$0.04 per kilowatt-hour levelized cost of electricity.

Project Approach

This project was led by a Sunpreme team developing and producing premium silicon photovoltaic panels that employ a unique glass-on-glass construction and heterojunction cell architecture with greater than 20 percent panel efficiency and industry-leading panel powers of greater than 400 watts per panel.

This project leverages the Sunpreme team's extensive knowledge of semiconductor and printed circuit board manufacturing. The team first tested and optimized processes on supplier equipment at the Sunpreme factory in China. Once the processes were well understood at pilot scale, the team built a fully integrated pilot line at the 10 to 15-megawatt scale in Sunpreme's Sunnyvale, California facility, then moved to a high-volume manufacturing environment in the United States. The Sunpreme project team, on-site design, research and development, and pilot manufacturing are headquartered in Silicon Valley. An additional 40-megawatt manufacturing facility is located outside the United States.

Project Results

The project team has demonstrated the process feasibility on individual tools at the China-based factory and begun the process of bringing the integrated toolset at Sunnyvale-based Sunpreme Research and Development center. The exposure tool with greater than 100-megawatt throughput capability has been ordered, installed and tested at Sunpreme.

By using the exposure tool, the team reduced the conducting finger width of the copper lines from 55 microns to less than 30 microns. They also developed a new patterning process that enabled a fine 20-micron narrow grid line resolution with an aspect ratio greater than 1.5:1. There was a 1 percent shadow loss reduction without increasing series resistance. Copper was proven to form a reliable contact between ribbon and bus bar with pull strength over 4 Newtons. The project team has achieved 24 percent PV cell efficiency with the newly optimized integrated process.

All the capital expenditure tools were quoted with 3,300 wafers per hour throughput. In the final analysis, the cost of a 150-megawatt copper line is \$0.022 per watt lower than silver line.

In effort to commercialize the developed technology. Sunpreme team selected a US-based manufacturing site and designed a detailed fabrication facility and layout, but unfortunately wasn't able to secure investment needed to realize the plan.

Advancing the Research to Market

Since several advanced silicon cell architectures are approaching the practical performance limits of silicon photovoltaic, the largest single improvement in the cost of domestic photovoltaic is a reduction in the materials and processing cost to fabricate those devices. Sunpreme's copper metallization technology will cut the consumable costs of advanced heterojunction cells by 53 percent, representing one of the most effective potential areas of innovation today. If the project can successfully demonstrate innovative manufacturing process for photovoltaic modules with 23% efficiency and secure investment for establishment

of commercial-scale operations in United States, it would catalyze massive growth of the domestic photovoltaic manufacturing industry.

The project team is a manufacturer of PV cells and modules, currently serving markets that include both rooftop and utility-scale applications. Sunpreme intends to commercialize its copper metallization technology and is committed to high-volume manufacturing of photovoltaic cells and modules in the United States using the process proposed in this project. If successful, Sunpreme's proposed copper-metallized cells will insert directly into the manufacturing toolset that could be established in US-based plant by 2020.

At the projected costs enabled by this project, Sunpreme expects that all planned domestic demand can potentially be supplied by domestically manufactured copper-plated heterojunction cells and panels, representing a serviceable available market of greater than 10 gigawatts per year.

Initially, this copper metallization innovation will establish a high-value product at low cost, creating a competitive advantage for Sunpreme. In the long-term, the technology will be applicable to all crystalline silicon photovoltaic cells, representing a transformational change in the way the photovoltaic industry metalizes cells. As a long-term strategy, Sunpreme and its partners intend to sell capital equipment and technology licenses to other domestic photovoltaic manufacturers. The wider use of this equipment and technology will result in significant performance and cost benefits across the industry. Collaborators will be the initial sales channel of these licenses, along with their tool sales; Sunpreme will also open licensing to other tool vendors. The primary market barrier to broad-scale application of this technology through a licensing model is validating the production costs and reliability of the approach. The demonstration of this technology, first under Solar Manufacturing Technology program and then through the project team's initial copper-plated products, is a prerequisite to demonstrating its value to manufacturing customers and overcoming that barrier.

Benefits to California

The key benefits to California ratepayers are threefold: (1) increased reliability of solar power generation assets and flattening of the solar power generation curve (or "Duck Curve") along with the enhanced grid stability that this flattening creates, (2) a decrease in environmental impact and emissions from power generated by clean-power technology improvements, and (3) increased employment, including more than 1,000 personnel directly associated with manufacturing operations in California by 2020, \$150 million in direct payroll, and an additional 3,000 indirect jobs once the manufacturing volume reaches the 1 gigawatt scale.

CHAPTER 1:

Introduction

This project “High-Performance Copper Plating for Heterojunction Silicon Cells, Based on Ultra-Low-Cost Printed Circuit Board Technology” is led by Sunpreme Inc., a manufacturer of premium silicon photovoltaic (Si-PV) panels that use a unique glass-on-glass construction and heterojunction cell architecture with power conversion efficiency greater than 20 percent from production panels and 22.5 percent from production cells. Sunpreme Inc. is headquartered in Silicon Valley with onsite design, research and development, and pilot manufacturing. Sunpreme Inc. also has a 40-megawatt (MW) facility in Jiaying, China. The tools developed by the project team are used in every semiconductor fabric in the world, and every integrated circuit chip made today has been processed using a tool designed by the project team.

As a manufacturer of low cost, high-performance solar cells, the project team has a distinct track record of success. More than 35 MW of Sunpreme’s hybrid cell technology cells have been integrated into PV modules and installed in the field to date. All of the project team’s products have a 20-year performance guarantee, backed by Munich Re, a major global insurance carrier.

Today 98 percent of all PV cells manufactured worldwide use silver for metallization. Silver paste is easy to work with but creates inefficiencies and increases costs. It is widely acknowledged that copper (Cu), at one-eighth the cost of silver, would be a better alternative. However, implementation of Cu patterning on silicon is currently cost prohibitive. To date, only California-based PV-panel manufacturer SunPower has Cu patterning capability. However, their manufacturing process remains expensive and the Cu-metallized cells are the most expensive PV cells for use in terrestrial modules. On the other hand, microelectronics manufacturers have established cost-effective use of Cu in ubiquitous applications such as printed circuit boards.

This project develops an innovative Cu metallization toolset and process that combines the high throughput and low-cost approach used in the printed circuit board industry with the more stringent specifications required for solar applications. In particular, the project team combines their hybrid cell technology with proven architectures from the microelectronics industry and develops a simplified toolset and process to pattern and deposit copper on Si-PV cells. This approach results in a 15 percent increase of power conversion efficiency, from 20.5 percent to 23.5 percent power conversion efficiency, while reducing cost below \$0.40 per watt peak (Wp). The advantages of copper patterning—narrower bus lines, lower resistivity, lower material cost—versus silver metallization enables this low cost, high throughput manufacturing, and will yield \$0.057 per kilowatt-hour levelized cost of electricity (LCOE) by 2019.

Measurement and Verification Plan

The project team continuously measured outcomes and verified results throughout the project. Table 1 shows how some general metrics were verified. Specific metrics are proprietary and not included in this application.

Table 1: Performance Metrics

Task	Metric	Method
Cells	<ul style="list-style-type: none"> • Cu line max height • Cu current density 	<ul style="list-style-type: none"> • 3D profilometer • IV Tester
General Process	<ul style="list-style-type: none"> • Batch Size • Wafer thickness • Breakage 	<ul style="list-style-type: none"> • Visual inspection • Micrometer
Lamination	<ul style="list-style-type: none"> • Placement • Film utilization 	<ul style="list-style-type: none"> • 3D profilometer • Optical map • SEM
UV Exp. Tool	<ul style="list-style-type: none"> • Min. line width: • Intra-wafer uniformity • Intra-batch uniformity 	<ul style="list-style-type: none"> • 3D profilometer • Optical map • SEM
Integration	<ul style="list-style-type: none"> • Full process throughput • Inter-batch uniformity 	<ul style="list-style-type: none"> • 3D profilometer • SEM
Production Qualification	<ul style="list-style-type: none"> • Cell Eff. • Panel Power • Panel Cost 	<ul style="list-style-type: none"> • IV-Tester/solar simulator AM1.5

Source: Sunprime, Inc.

CHAPTER 2:

Project Approach

The project is structured around five technical tasks, which are described in this section. To simplify cross-referencing, the numbering of the tasks used in this chapter matches that in the Statement of Work and other project documents.

The project team has completed or made significant progress on tasks 2, 3, 5, and 6. The tabularized summary of the tasks is given in Table 2.

Task 2: Process Development and Tool Specifications

The goal of this task was to modify a commercial laminator, automation equipment, dual-sided exposure tool for high-throughput wafer patterning, and process module for developing the dry-film resist from the printed circuit board industry to process heterojunction cells in batches of a minimum of 12 wafers (3x4 array) with the required throughput, breakage, and lamination yield. The project team worked with tool suppliers to establish a final specification for each ordered process tool and execute an agreement that will lead to 25+ MW of United States (US) manufacturing capacity based upon the toolsets and processes developed in Tasks 2 through 4 of this project.

Task 3: Tool Ordering, Installation, and Testing

The goal of this task was to order the exposure tool, plating tool, laminator, stripping tool, etching tool, and inter-tool automation equipment with the purpose of designing and implementing upgrades to the Sunprime's pilot facility. After installation of ordered tools, the project team developed baseline process modules for back-end process steps including separating wafers from the carrier.

Task 4: Process Integration and Optimization on Pilot Line

The goal of this task was to execute a contract with an investor and secure funding for establishment of an US-based 300 MW solar manufacturing facility where the developed toolset and processes could be integrated into a high-volume throughput production line.

Task 5: Techno-Economic Production and Cost Models

The major goal of this task was to collect all production and field data during the project duration and to create techno-economic models of the complete manufacturing process. These models were used to estimate operating costs at a range of production volumes and to demonstrate that the final process can meet project targets at scale.

Task 6: Evaluation of Project Benefits to California Investor-Owned Utility Ratepayers

The goal of this task was to describe and report the ratepayers benefits from this project.

Table 2: Detailed List of Project Tasks/Subtasks

Task/ Subtask #	Task/Subtask Name	Meeting Name	Product(s)
2	Process Development and Tool Specifications		Draft Process Development and Tool Specifications Report Final Process Development and Tool Specifications Report Copy of Agreement for United States Manufacturing Facility
3	Tool Ordering, Installation, and Testing	Critical Project Review #1	Draft Tool Ordering and Installation Report Final Tool Ordering and Installation Report Business Development Report Copy of Third-Party Test Results Critical Project Review Report
4	Process Integration and Optimization on Pilot Line	Critical Project Review #1	Draft Process Integration and Optimization on Pilot Line Report Final Process Integration and Optimization on Pilot Line Report Copies of Master Supply Agreements Critical Project Review Report
5	Techno-Economic Production and Cost Models		Draft Techno-Economic Production and Cost Models Report Final Techno-Economic Production and Cost Models Report
6	Evaluation of Project Benefits		Kick-off Meeting Benefits Questionnaire Mid-term Benefits Questionnaire Final Meeting Benefits Questionnaire

Source: Sunpreme, Inc.

CHAPTER 3:

Project Results

Task 2. Process Development and Tool Specifications

The goals of this task were to modify a commercial laminator, automation equipment, dual-sided exposure tool for high-throughput wafer patterning, process module for developing the dry-film resist from the printed circuit board industry to process heterojunction cells in batches of wafers with the required throughput, and breakage and lamination yield. To that end the project team successfully completed the following subtasks:

1. Design, development, and test of wafer carrier
2. Demonstration of wafer carrier ability to meet minimum requirements for high volume manufacturing
3. Development of specifications for lamination process
4. Development of specifications for etching and stripping processes
5. Development of specifications for the exposure tool, plating tool, laminator, stripping tool, etching tool, and inter-tool automation equipment

Subtask 1. Design, Development, and Test of Wafer Carrier

This task involved three steps:

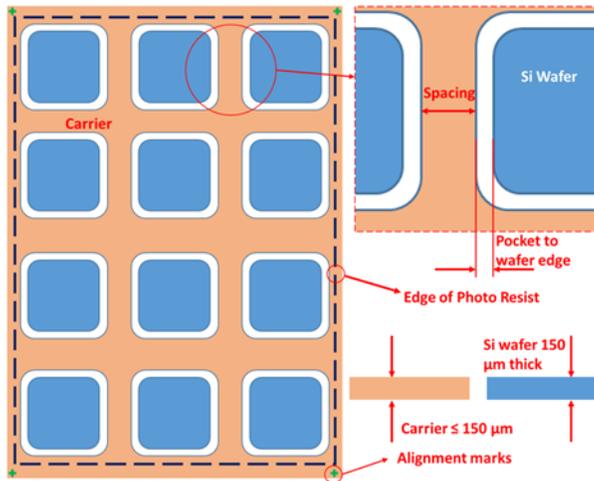
- Assessment of the impact of carrier thickness and gap size on dry-film use and wafer alignment, using a straight-edge model
- Assessment of the reliability of physical registration versus optical alignment to fiducials on the wafer carrier versus optical alignment to individual wafers using two wafer carriers built by the project team
- Test of post-lamination rigidity of wafer carrier

During this subtask twenty-four wafer carrier designs were tested, which considered four different pocket widths, three different carrier thicknesses, and two different structural widths (Figure 1).

The dark line in the left image in Figure 2 demonstrates a 500 micrometer (μm) thick carrier with a significant airgap between carrier and wafer edge post-lamination. This suggests the resist film is not sealing at the edge in the thick carrier instance. In comparison, the dark line is absent in the images in the center and on the right in Figure 2, meaning, that 100 μm and 150 μm carriers did not form air pockets on wafer edges.

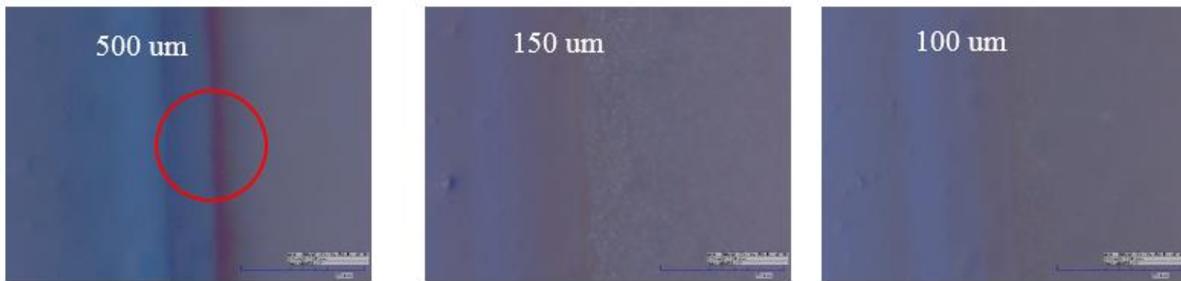
Figure 3 shows that during development, wafers came loose from 100 μm carriers. It would potentially cause automation problems in the future of high-volume manufacturing. Therefore 150 μm carriers have the most suitable size for the process developed under this project.

Figure 1: 4x3 Carrier Design Calculation



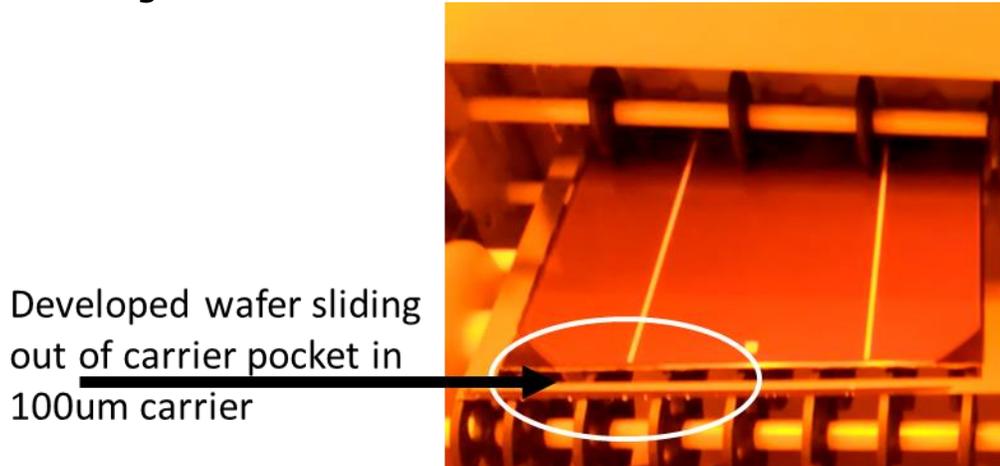
Source: Sunpreme, Inc.

Figure 2: Air-Gap Post-Lamination



Source: Sunpreme, Inc.

Figure 3: Unsecure Wafer Connection to Carriers



Source: Sunpreme, Inc.

In the next step wafers, were hand-placed in carriers within the tolerance limits of allowable x-y motion regarding to the optimal placement and laminated (Figure 4 and Figure 5). The maximum allowable movement along either x or y axis was 2mm, and maximum allowable angle for wafer rotation was 1 degree. The following results show that the wafer movement during lamination process was well within qualifying requirements:

- Mean x-y motion = 0.1mm
- x-y standard deviation = 0.05mm
- Mean rotational deviation = 0.1°
- Rotation standard deviation = 0.06°

Figure 4: Grids Drawn on Dry Film and Carrier Before Lamination



Source: Sunpreme, Inc.

Figure 5: Post-lamination Measurements Within Expected Tolerances

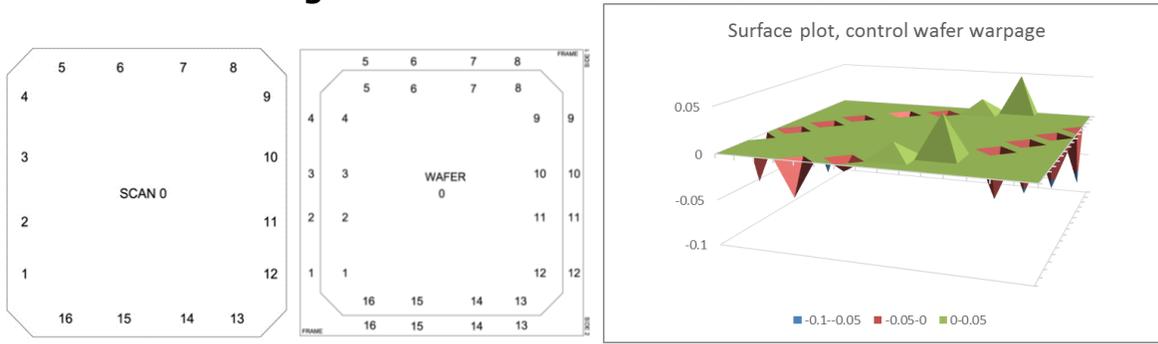


Source: Sunpreme, Inc.

Post-lamination rigidity of the wafer carrier was tested on ten wafers. All wafers were measured after before and after they were laminated into a single-wafer carrier. Wafer lift was measured at 16 points on the wafer against a reference plane and an additional 16 points on the carrier (Figure 6). The maximum allowable physical lift of wafers was 500 μm . The following results were achieved and show satisfying lift control (230 μm):

- Maximum lift (wafer) = 230 μm mm
- Median lift = 50 μm (wafer)
- Standard deviation = 50 μm (wafer)
- Maximum lift (carrier) = 380 μm
- Median lift = 90 μm (carrier)
- Standard deviation = 70 μm (carrier)

Figure 6: Measurements of Ten Wafers

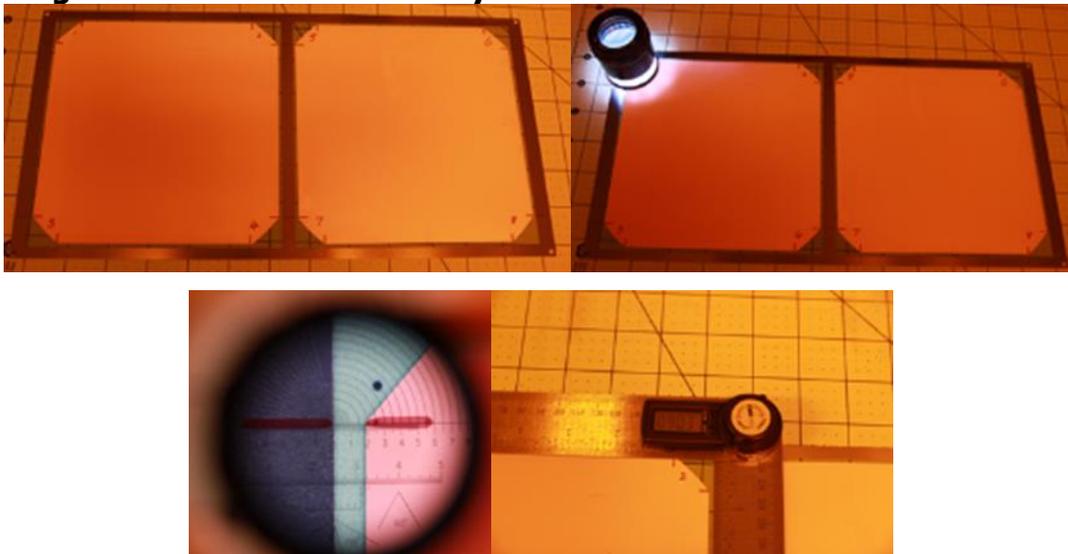


Source: Sunpreme, Inc.

Subtask 2. Demonstration of Wafer Carrier Ability to Meet Minimum Requirements for High Volume Manufacturing

The goal of this subtask was to limit the wafer movement during lamination process to the maximum of 500 μm in either x or y-axis direction and the wafer rotation to the maximum of 1° . The project team and a vendor evaluated 10 wafers at four different points each and extrapolated the tilt angle from the x-y measurement. First, the grids were drawn on the dry film and carrier prior to lamination, as shown in Figure 7.

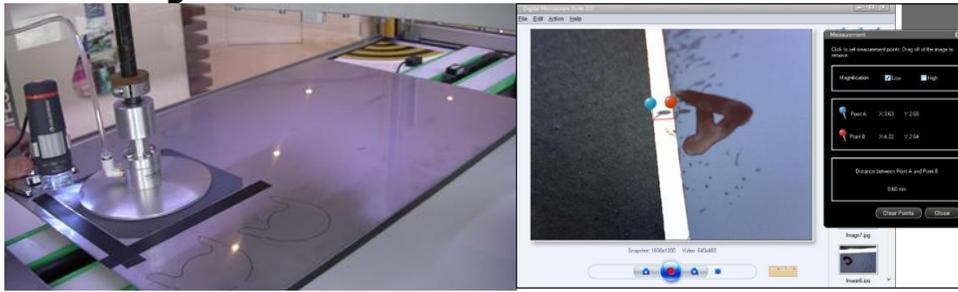
Figure 7: Grids Drawn on Dry Film and Carrier Before Lamination



Source: Sunpreme, Inc.

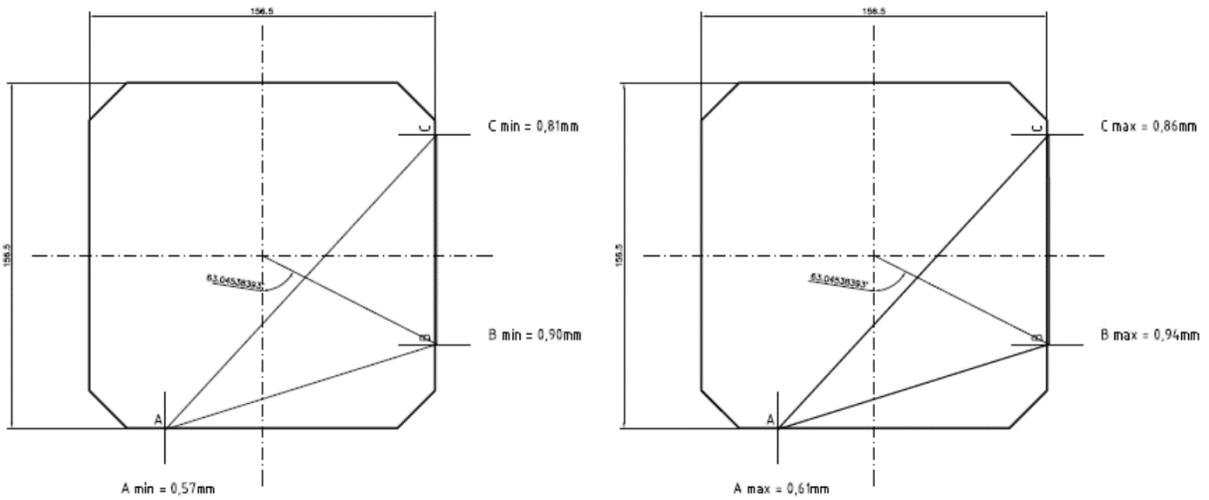
To test the ability of the wafer carrier to place wafers in the targeted positions, a robotic arm equipped with a lamp was used (Figure 8). The robotic arm picked up and transferred wafers between positions 10,000; no breakage of wafers was observed. Ten measurements were done on three locations on the wafers. The maximum x-y delta didn't exceed 50 μm . The rotation was less than 0.001° between maximum and minimum dislocation comparison, as shown in Figure 9. Table 3 summarizes the results from the ten measurements.

Figure 8: Wafer Transfer Between Positions



Source: Sunprime, Inc.

Figure 9: Maximum and Minimum Deviation of Positions A, B, and C Input into AutoCAD



Source: Sunprime, Inc.

Table 3: Ten Measurements on Three Locations of Wafers

Test	Position A	Position B	Position C
1	0.58	0.94	0.81
2	0.57	0.91	0.84
3	0.59	0.91	0.84
4	0.60	0.90	0.85
5	0.61	0.91	0.84
6	0.58	0.92	0.81
7	0.60	0.93	0.85
8	0.59	0.91	0.85
9	0.59	0.90	0.82
10	0.59	0.91	0.86
Min Value	0.57	0.90	0.81
Max Value	0.61	0.94	0.86
Delta	0.04	0.04	0.05

Source: Sunpreme, Inc.

Subtask 3. Development of Specifications for Lamination Process

The goal of this subtask is the development of various lamination specifications that would qualify for vendor capability at the vendor’s site. The lamination operation limits are as follows:

- Maximum variation of temperature within the chamber must not exceed 5°C (41 F)
- Maximum time the lamination chamber at 1millibarr (mbar) cannot exceed 20 seconds
- The chamber must have yield of more than 95 percent and a throughput of 300 wafers per hour (WPH)

The team measured the temperature of each evaluated wafer at five different points (cardinal points plus center and then repeated these measurements for another five different temperature settings in the range of 30°C to 80°C (86 – 176 F), as shown in Table 4. Wafer temperatures were measured by using a KEYENCE data logger and nine thermocouple type T tapped to the substrate. With a pump down time of 5 seconds plus vacuum time of 30 seconds plus slap down time of 10 seconds, the total process time per batch lasted 50 seconds, including loading and unloading. With 12 wafer carriers, throughput this time converts to approximately 860 WPH. The results of the measurements are summarized in Table 4. Figure 10 shows that all twelve wafers were laminated with no failure — no breakage, bubbles, wrinkles, or pin holes. The maximum temperature variation was $\pm 3.68^{\circ}\text{C}$ (± 6.62 F).

Table 4: Temperature Measurements for Each Temperature Setting

Set Points °C	1	2	3	4	5	6	7	8	9	Max ΔT
40	39.62	41.31	41.02	39.48	41.41	40.32	40.33	41.06	41.30	1.93
50	49.52	51.53	50.93	49.60	51.72	49.92	50.37	51.10	51.46	2.20
60	61.09	61.90	61.52	59.36	62.24	61.67	60.95	62.59	62.38	3.23
70	69.90	71.96	71.41	69.74	72.12	70.82	70.60	72.45	72.48	2.74
80	80.14	82.37	81.01	79.05	82.31	81.07	80.62	82.73	82.50	3.68

(50°C is Baseline)

Source: Sunpreme, Inc.

Figure 10: Measured Wafer Temperature and Nine Thermocouple Type T Tapped to the Substrate



Source: Sunpreme, Inc.

Subtask 4. Development of Specifications for Etching and Stripping Processes

The goal of this subtask is to develop specifications for etching and stripping processes that would qualify for vendor capability at the vendor's site.

For stripper specification the set requirement is the absence of visible photo resist residue on 10 or more test samples randomly selected after they have been through the photo resist process with an expected throughput of 300 WPH. For evaluation, the selected stripper wafers were visually inspected for photo resist residue on a three-lane system with a conveyor speed at 36 inches per minute. The inspection throughput, therefore, was equal to 790 WPH. A total of sixteen wafers was evaluated; none of them had visible post photo resist residue.

For etcher specification the set requirement is the absence of visible copper residue for at least 10 samples selected from etching process executed with throughput speed of 300 WPH. For the determination whether this specification was achieved for the developed etching process, sixteen wafers were visually inspected for copper residue post etch on a conveyor with a throughput speed of 490 WPH. None of the inspected wafers had visible copper residue.

Subtask 5. Development of Specifications for the Patterning Process, Exposure Tool and Inter-tool Automation Equipment

To determine whether or not the patterning process and the exposure tool would meet the specifications are in agreement with the vendor’s capability, ten wafers were exposed and developed using the vendor’s demonstration tool. The post-development patterning trench opening profiles were measured by an in-house 3D microscope, as shown in Figure 11. The width of open trench was measured at 4 different positions C1-C4 as well at the center and at the place of maximum width of open trench between copper “fingers” and the quantitative data are summarized in Table 5.

Figure 11: Post-Development 3D Microscope Image of Open Trench between Copper “Fingers”



Source: Sunpreme, Inc.

Table 5: The Widths Data of Open Trenches for Ten Wafers

Wafer ID	3450	3454	3456	3458	3460	3487	3502	3504	3506	3509
C1	46.64	48.46	48.48	46.34	46.53	46.12	46.02	46.54	47.43	48.49
C2	46.64	48.18	47.91	46.24	46.54	46.19	45.99	48.19	47.24	49.01
C3	47.3	46.27	47.11	46.8	47.39	46.29	45.99	49.01	46.52	47.91
C4	46.86	48.18	48.57	46.26	46.53	46.92	46.52	47.1	47.07	48.54
Center	46.74	48.21	47.38	46.54	45.99	45.06	44.86	47.39	47.35	40.02
Max	47.3	48.46	48.57	46.8	47.39	46.92	46.52	49.01	47.43	49.02
Average	46.84	47.86	47.89	46.44	46.60	46.12	45.88	47.65	47.12	48.59
Std Dev	0.246	0.802	0.580	0.211	0.449	0.600	0.547	0.865	0.324	0.409
2 Sigma	1.0%	3.4%	2.4%	0.9%	1.9%	2.6%	2.4%	3.6%	1.4%	1.7%

Source: Sunpreme, Inc.

Quantified outcome:

- Exposure time was less than 2 seconds, including manual loading and unloading less than 40 seconds
- Mean width = 47.1 μm
- Maximum width = 49.02 μm
- Mean Two Sigma (2σ) = 2.2 percent with maximum = 3.6 percent

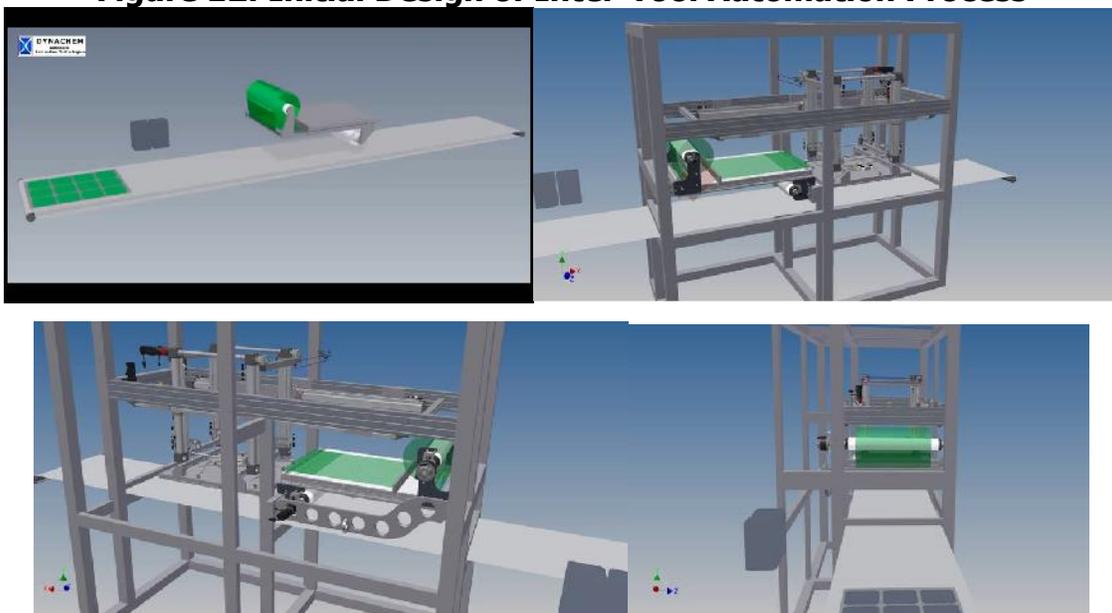
The following conclusion was made after the evaluation of PV cells performance with open trench widths provided in Table 4:

- Short-circuit current density is lower than previously obtained results for the PV cells with silver patterning due to wider open trench between copper "fingers"
- Different vacuum levels during the exposure process (800 mbar vs 1000 mbar) resulted in similar performance of the exposure tool
- Patterning process with narrower width of open trench between copper "fingers" (45 μm) must be designed and tested next

Based on the conclusions, the design for patterning process has been optimized to apply narrower copper "fingers" with narrower open trench on the silicon surface of the PV cells. After the PV cells with new copper patterning design were developed in the exposure tool, the measured the width of open trench was around 42 μm . The measured short-circuit current density was higher than previously obtained results for the PV cells with silver patterning.

The initial design of inter-tool automation process is shown in Figure 12. Here the silicon wafer was picked up from the automation lane and transported to the laminator tool for double-sided lamination. Key requirement for this step is the precise sheet placement on the carrier in accordance with developed specifications for lamination process as described in the subtask 1.

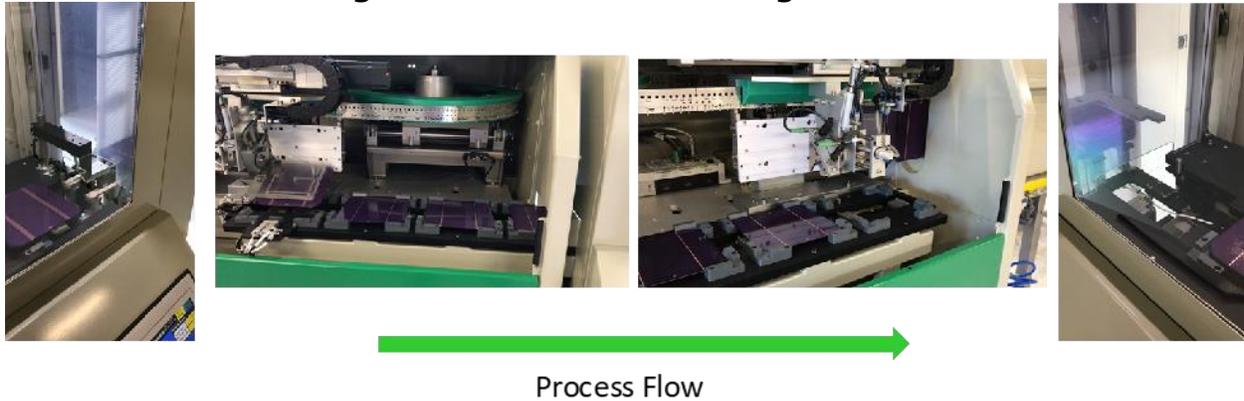
Figure 12: Initial Design of Inter-Tool Automation Process



Source: Sunpreme, Inc.

The installed automated plating pilot plating line is shown in Figure 13.

Figure 13: Automated Plating Process



Source: Sunpreme, Inc.

Task 3: Tool Ordering, Installation, and Testing

The goal of this task was to order the exposure tool, plating tool, laminator, stripping tool, and etching tool; develop inter-tool automation; design and implement upgrades to the project's pilot facility; meet all requirements for delivery and installation of ordered tools; install the complete toolset; and develop baseline process modules for back-end process steps including separating wafers from the carrier.

The project team partially completed the following tasks:

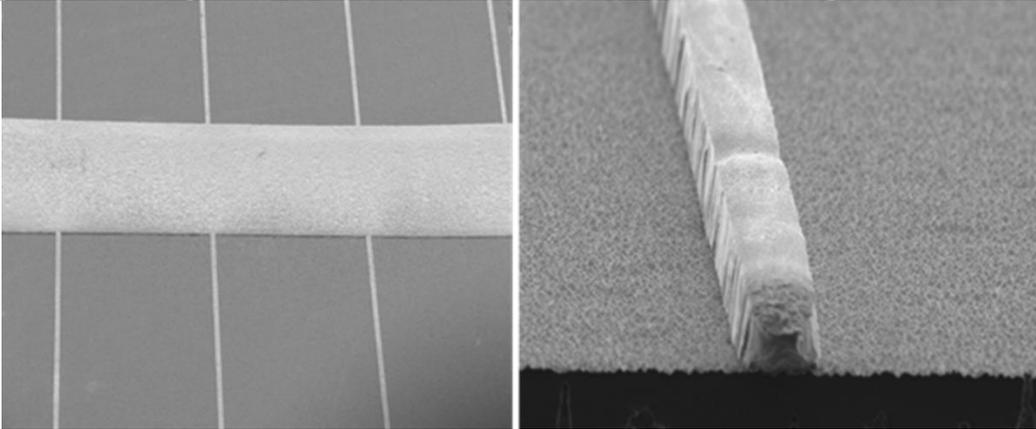
- Exploration of different vendor sites and identification of potential supplier and customer sites
- Ordering of plating tool, exposure tool, laminator, developer, stripper, etcher, automation. Project team has ordered a high-volume manufacturing scale exposure tool
- Fitting-up of pilot facility to receive ordered tools
- Installation of high-volume manufacturing-capable vacuum laminator, exposure tool, developer, plating tool, stripping tool, etching tool; automation in project team's pilot facility; and optimization of the baseline process modules for each tool. The exposure tool was installed and tested.
- Fabrication of 10 test cells using the carrier, in-house tools, and vendor supplied demos tools
- Preparation of 12 copper metallized modules for third-party that were tested by Fraunhofer in compliance with the Underwriters Laboratories and International Electrotechnical Commission standards

Single achievements are summarized below:

- High resolution UV exposure tool (~150 MW capacity) was installed and project team developed an innovative patterning process enabling a fine 20 μm narrow grid line resolution with aspect ratio (height: width) over 1.5:1 as shown in Figure 14. As a result, there was a 1 percent shadow loss reduction while resistance remained at the same level. It was proven that copper can form a reliable contact between ribbon and

bus bar with pull strength that is measured on pulling the bus bar off the cell over 4 Newtons.

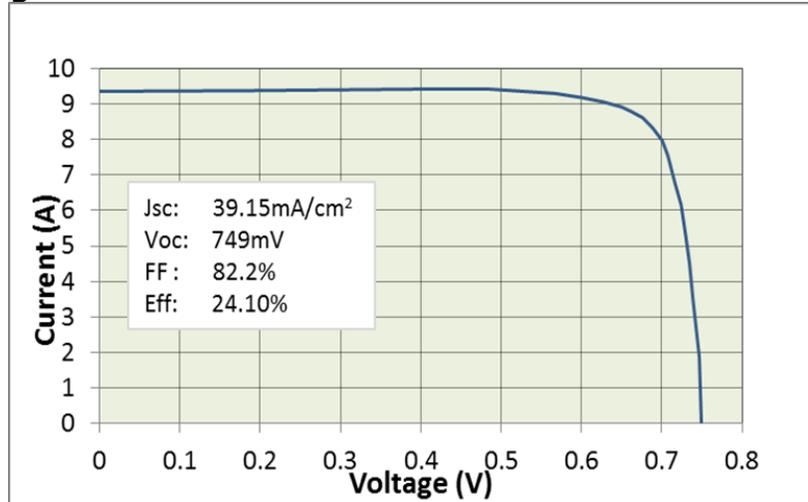
Figure 14: 20 μm Narrow Grid Line Resolution with Aspect Ratio 1.5:1



Source: Sunpreme, Inc.

- Using the innovative optimized process, project team produced silicon-PV cells with copper metallization featuring 24 percent cell efficiency as indicated in Figure 15.

Figure 15: Achievement of 24.1 Percent Cell Efficiency



Source: Sunpreme, Inc.

- A factory site was selected for integrated 300 MW cell and module manufacturing, where the developed tools and processes could be used to invigorate solar manufacturing in the United States, as visualized in Figure 16.

Figure 16: Prototype Factory Site



Source: Sunprime, Inc.

- A 300-MW copper cell/module production layout was designed

Task 4: Process Integration and Optimization on Pilot Line

The project team engaged in market outreach to project financiers, utilities, independent power producers, and non-utility generators to help these parties of the generation ecosystem understand the long-term financial effect of panel selection decisions. The project team secured its first 30-year, third-party warranty on a panel, issued by Munich Re, a large re-insurer, with a history of conservative investments in insurance and warranty products. The project team also signed a major (150 MW) multi-year supply agreement with a major customer. However, the global downturn of the solar industry increased the perceived investors risk and the negotiations with some large investors didn't result in a signed contract. Therefore, the project team was unable to secure enough capital to cover capital expenditure (CAPEX) cost for a large-scale manufacturing facility as required under Task 4.

Task 5: Techno-Economic Production and Cost Models

The goal of this task is to combine all production and field data collected during this project and create techno-economic production and cost models describing the complete manufacturing process. These models enable cost projections depending on production volumes and demonstrate that the final process can meet project targets at scale.

To that end the project team successfully completed the following tasks:

- Development of production and cost models for the high volume manufacturing toolset
- Integration of the results from Task 4 to refine the cost models and calculate the module production costs at a throughput of 300MW/year.
- Preparation of the "Techno-Economic Production and Cost Models Report" submitted to the Energy Commission as a part of Task 5 Deliverables.

Single achievement included:

- The high-volume manufacturing copper toolset was quoted at 150 MW per unit line. A detailed cost analysis based on 300 MW of capacity showed the total cost for a module with copper patterning is \$0.022 per watt, which is lower than the total costs of a module with silver patterning.

Task 6: Evaluation of Project Benefits to California Investor-Owned Utility Ratepayers

The production tools and processes developed during this project would allow to manufacture 400W heterojunction PV panels with the module efficiency of 23.5 percent and at a cost of less than \$0.40 per watt. Thus, the current balance of system costs outlined in the funding opportunity announcement DoE FOA EE0001400 would be reduced due to the higher efficiency/higher power of the manufactured solar panels and translate into the levelized cost of electricity of \$0.57 per kilowatt-hour.

The unique heterojunction design of photovoltaic cells combined with the compound thin-layer architecture and high-quality manufacturing process would slow light-induced degradation of the manufactured cells significantly. Hence, PV cells manufactured during this project were warranted at less than 0.6 percent annual degradation. In contrast today's low-cost polycrystalline silicon modules can lose 1 to 2 percent of power conversion efficiency per year; the industry standard warranty is 1.2 percent annual degradation.

In addition, the double-glass module technology eliminates the need of back sheet, which reduces potential fire hazard. Also, lower production costs estimated for high throughput manufacturing of the developed PV cells with copper patterning will accelerate California's transition to carbon-neutral electricity system by 2045 and help in meeting the state's emission reduction goals.

CHAPTER 4:

Technology/Knowledge/Market Transfer Activities

Technology Transfer to Market

In addressing the decline of photovoltaic manufacturing in the United States, which has been dramatic and can be attributed primarily to the rapid reduction of silicon module costs internationally, the project team aims to create a robust presence in the United States and establish a domestic manufacturing using the technical advancements achieved under this project.

Establishment of domestic manufacturing of solar technologies also has important ancillary effects, such as the development of domestic supply chain and other supporting industries. Initial support to this project from the Office of Energy Efficiency and Renewable Energy and through their Solar Manufacturing Technologies (SolarMAT) program is a vital linchpin in the project team's domestic expansion strategy. This overall effort could serve as the template for federal engagement to work in partnership with multiple state and municipal organizations to revamp the United States' advanced manufacturing capabilities.

The project team is a cell and module manufacturer that intends to bring the technology developed under this project to the domestic market. The team is committed to development of high-volume manufacturing in the United States of PV cells and modules using the copper metallization process proposed in this report. If the results of this research are adopted, the developed copper-metallized PV cells will be fabricated using the designed and tested manufacturing toolset.

The project team's current markets for the developed product includes rooftop and utility-scale solar installations, with about 75 percent going to rooftop due to the inherent value of higher efficiency panels. At the projected costs enabled by the project funded by SolarMAT program and co-funded by the California Energy Commission, all planned domestic demand can potentially be supplied by domestically manufactured copper-plated heterojunction cells and panels.

Currently, several advanced silicon PV cell architectures are approaching the practical performance limits. Hence, the largest single improvement in the cost of domestically produced PV panels can be achieved through cost reduction of used materials and decreasing of the processing cost to fabricate those devices. The manufacturing approach developed for this project has the potential to decrease the consumable costs of advanced heterojunction cells by 53 percent, representing one of the most effective potential areas of innovation today. The know-how from this project can catalyze massive growth of the domestic PV manufacturing industry. Initially, this innovation would create a high value product at low cost. In the long-term, the technology could be applicable to all crystalline silicon PV cells and transform the way the PV industry metalizes solar cells. As a long-term strategy, technology licenses can be sold to domestic PV manufacturers, enabling a wide acceptance of the

developed innovative solution. The resulting significant performance and cost benefits could boost the entire solar industry in the United States.

The primary market barrier to broad-scale application of this technology through a licensing model is the ability to validate the production costs and reliability of the approach. The demonstration of this technology, first under SolarMAT and EPIC programs and then through commercialized copper-plated solar products, is a prerequisite to demonstrating its value to manufacturing customers.

Result Dissemination

The project team presented results to academia and industry through presentations and publications:

- Presentation at 2017 Intersolar: "Sunpreme's compelling hybrid cell technology-Based Bifacial PV solutions for the Commercial and Industrial Space"
- Presentation at 2017 SPI: "Sunpreme's Cu Metallized hybrid cell technology Cell & 410W Module"
- Presentation at 2018 EPIC Symposium: "High Performance Cu-Plating for Heterojunction Silicon Cells, Based on Ultra-Low-Cost Printed Circuit Board (PCB) Technology"
- Publication and presentation at WCPEC-7, WAIKOLOA, HAWAII, June 10-15, 2018: "Efficiency Hybrid Cell Technology Integrating a Low-cost, Precision-Pattern Cu Metallization Used for Advanced PCB".

CHAPTER 5:

Conclusions/Recommendations

The project team did not experience any unexpected technical challenges that could not be resolved. The major obstacle is related to the situation on the solar market. Globally, photovoltaics and solar power have been in a down cycle since early 2015. This downturn, coupled with a significant overbuild of capacity by Chinese module makers has led to a huge oversupply of panels on the global market. The result of the oversupply is that panel prices have dropped by approximately 15 percent during the last 12 months in accordance with the law of supply and demand.

In even the most conservative scenarios, the industry expected solar markets to follow the same up-and-down pattern as computer memory markets, with peaks and valleys lasting approximately 18 to 24 months, and investment cycles following a similar period. However, thus far, this downturn has lasted four years and has had the effect of drying up investment capital, particularly for capital-intensive operations like building a lab for solar cell and module manufacturing.

The specific challenge to the project team has been in closing an investment deal that would secure enough capital to establish a manufacturing line in the United States (Task 4). Although the several investors indicated interest financing the developed technology, they did not follow through because of the industry downturn. The changes to the Section 201 (<https://www.seia.org/research-resources/section-201-solar-tariffs>) and Section 301 Tariffs (<https://www.strtrade.com/f-tariff-actions-resources.html>) that came into effect in February 2018, include trade decisions to tax sales of the overstocked inventories from China, including solar cells and modules. However, instead of an expected boost to the domestic solar manufacturing, the announcement of the Section 201 and 301 decision made it extraordinary difficult for the project team to get a term sheet ready for a significant customer financing round. After months of negotiations with few potential investors no deal for financing of new PV manufacturing plant in the United States has been closed. Therefore, Sunpreme was not able to complete Task 4 due to the time and financial constraints..

As the project demonstrated, there is no technical risk to scaling from pilot-scale manufacturing to high throughput manufacturing with a capacity greater than 100MW. Some potential challenges include process optimization, and inter- and intra-tool automation to ensure highly automated production processes within each individual tool and the entire tool set. To minimize the risk of automation challenges, the project team demonstrated automation solutions on a smaller scale using tools and equipment that would be used on a commercial-scale. Key advantages of the developed manufacturing process include the consistent ability to achieve 99 percent yields in volume manufacturing (compared with 50 to 60 percent yields at Asian polycrystalline-silicon cell labs), glass-on-glass packaging architecture that eliminates the most common failure mode (back sheet failure) for solar modules, and heterojunction cell architecture, which eliminates light-induced degradation common to Passivated Emitter and Rear Cell (PERC) cells. The total of these advantages means that produced copper-patterned cells and modules are reliable and could potentially match the 50- to 60-year replacement

cycle for steam turbines and other traditional power generation equipment and still be at greater than 90 percent of their nameplate generation capability.

Regarding commercialization of the technology developed under this project, the major obstacle was securing an investment large enough to cover capital expenditure (CAPEX) costs required for a factory located in the United States. With no investor commitment, the project team had to wind down its California-based Research and Development activities as of April 2019 and most of the team members have moved to different companies.

Although the project team's advanced hybrid cell technology with copper metallization could provide the ratepayers benefits of lower costs and greater reliability of electricity generation, improved air quality due to reduction of climate pollutant emissions, and creation of job opportunities, establishment of manufacturing in the United States is not possible without major investment.

CHAPTER 6:

Benefits to Ratepayers

Ratepayer Impacts

The greatest single impact this project will have on California ratepayers comes in the form of lower cost for modules, and ultimately lower cost for electricity. Costs are described below. Reliability is a close second, however.

Cost Reduction

If successful, the production tools and processes developed here will allow Sunprime to manufacture volume HTC cells at 23.5 percent efficiency and 400W panels at a cost less than 40¢/W. Using 2014 BOS costs outlined in the DoE FOA EE0001400, combined with the reduced BOS cost resulting from our higher-efficiency/higher-power panels, the products enabled by this project will support a levelized cost of electricity of 5.7¢/kWh by 2019. This exceeds the Department of Energy/Office of Energy Efficiency and Renewable Energy target of 6¢/kWh by 2020, by 5 percent, fully one year ahead of schedule. If the Department of Energy is also successful in achieving their independent target of BOS costs less than 50¢/W, then, combined with the products resulting from this project, we have the potential to achieve a levelized cost of electricity of 3¢/kWh by 2030.

Given a 10 percent guaranteed return to the Investor Owned Utilities, a 3¢/kWh levelized cost of electricity suggests that California Investor Owned Utilities will be able to add gigawatts of peak-demand production capability at a cost to ratepayers of less than 4¢/kWh, as opposed to bottom-tier PG&E rates of 19.5¢/kWh under the recently approved 2-tier rate structure as of January 2019.

Reliability

The unique hybrid cell technology architecture and high-quality manufacturing mean that developed cells have virtually no light-induced degradation – we warranty them at better than 0.6 percent annual degradation. In contrast today's low-cost poly-crystalline Si modules can lose 1-2 percent of power conversion efficiency per year; the industry standard warranty is 1.2 percent annual degradation. To compare the two, at 1.2 percent degradation, a 10kW system built with 16 percent efficient Trina panels would produce 80 percent of the nameplate (8kW) and operate at 12.7 percent efficiency after 20 years in the field. A similar Sunprime system would produce 9kW with 19.2 percent efficiency after 20 years. Considering a lifetime consistent with other utility-scale generation equipment, the effect is even more pronounced, with the Sunprime system producing 7kW at 15 percent efficiency after 60 years in the field. The Trina system, were it even still operational, would produce less than 5kW at 7.8 percent efficiency under the same conditions.

Greenhouse Gas Emission Reduction

Replacement of all coal, gas and petroleum fired electricity production with solar electricity generation would reduce California GHG emissions by millions of Metric tons annually, a significant step towards California's greenhouse gas reduction and clean energy goals.

Market Impact

The target is high-volume production of 23 percent efficient, 400W, 72-cell panels with a production cost of less than 40¢/W that sell at 20 percent margins (50¢/W). In contrast, today's state of the art utility-scale PV panels are 21.5 percent efficient, 345W, 96-cell panels from SunPower that sell at 75¢/W with 10 percent margins. The panels can succeed in the marketplace due to their lower price and superior performance.

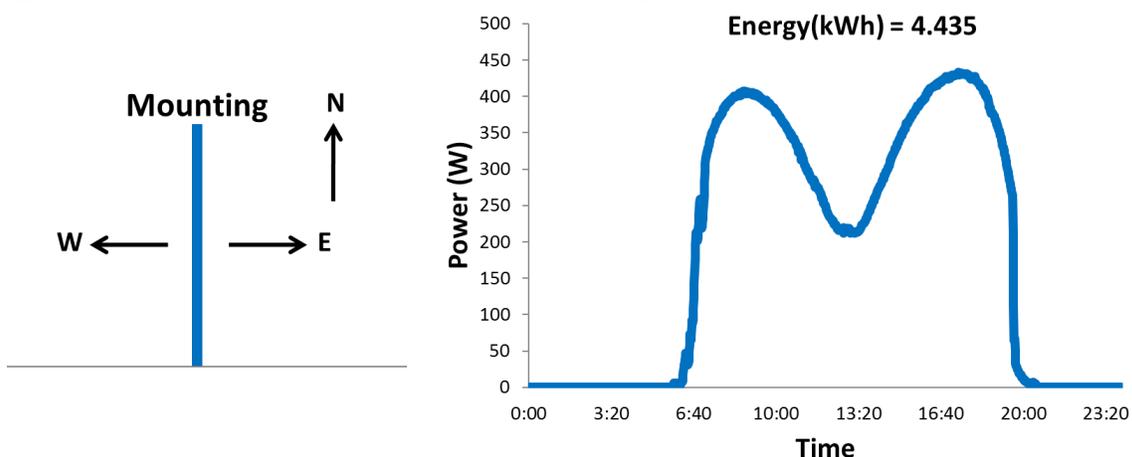
Ratepayer value estimates are based on the assumption of market adoption of the proposed Cu-plating technology.. As a long-term strategy, Sunprime and its partners intend to sell capital equipment and technology licenses to other PV manufacturers, so that this solution can be widely used. Broad market adoption within an additional 5 years would result in substantial performance and cost benefits across the entire industry.

Unique Bi-Facial Module for Glass-on-Glass Integration

Due to the unique features of the bi-facial module, the "Duck Curve" effect (imbalance between energy generation and peak demand during early morning and early afternoon) is reduced. The hybrid cell technology modules "wake up" earlier in the morning and, by the same token, "go to bed" later in the afternoon due to better "Low Light Performance" as a result of higher open circuit voltage. The modules can be mounted vertically such that a double hump can be achieved in the energy generation curve as well as an increase in integrated power (area under the curve) generation. There is less than a 10 percent efficiency difference between the front side and backside of the modules. Therefore, with equal irradiation the power generated from "Sunny Side up" vs. "Sunny Side Down" is only 5-10 percent.

The project team developed the bi-facial design to enable vertical installation and achieve "double humps" of power output during the day. Figure 17 and Table 6 show the total power output of a vertically installed Sunprime 500W bi-facial module as well as peak power output from each side of the module.

Figure 17: Power Output from a Vertically Installed 500W Bi-facial Module



Source: Sunprime, Inc.

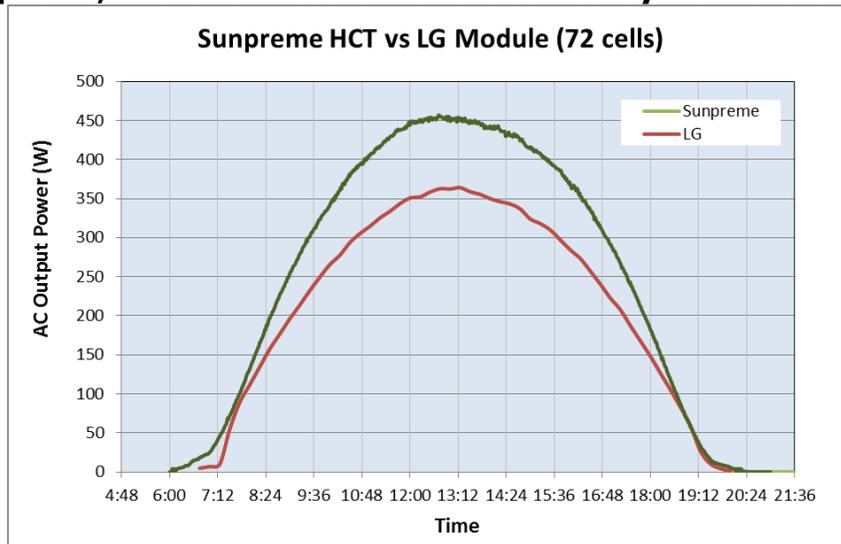
Table 6: Peak Power Output from Both Sides of the Module

90 Analysis	Energy (kWh)	Energy %	Peak Power (W)	Time of Peak Power
East Half	2.075	47%	407	8:44AM
West Half	2.360	53%	433	5:22PM

Source: Sunpreme, Inc.

Figure 18 shows the project team’s copper module produces 95 W more AC power compared with the module manufactured by LG Electronics, Inc. under the same radiation conditions.

Figure 18: Power Output of Bi-facial Hybrid Cell Technology for Module developed by Sunpreme, Inc. and Module manufactured by LG Electronics, Inc.



Source: Sunpreme, Inc.

In one project team’s 5MW ground mount installation the modules generated 9.5 GWh annually, equal to 285GWh in its lifetime. This is a considerable improvement compared to 172GWh lifetime generation with a competitor’s 5MW installation. This corresponds to 24 percent greater annual energy production over the competitor. In other words, this allows customer monetization and lifetime revenue of \$23 million from Sunpreme modules versus \$15 million revenue from competitors’ modules. Table 7 shows the project team’s bi-facial module has a levelized cost of electricity at USD 1.695 cents/kWh which is 22 percent better than the competitor’s mono facial module.

Table 7: Comparison Between the Project Team Bifacial and Solar Competitor's Mono Facial Modules

	Company X Mono facial product 325W	Sunpreme 370W
Estimated System Size (W):	5,000,000	5,000,000
# Modules Required	15,385	13,513
Bifacial Boost	None	With Backside Boost
Module Value (\$/W)	\$0.38	\$0.58
BoS Cost (\$/W)	\$0.34	\$0.27
Inverter	\$0.09	\$0.09
Racking	\$0.05	\$0.04
BOS -Electrical/Mechanical	\$0.08	\$0.05
Labor	\$0.08	\$0.05
Design, Permitting, EPC OH/Profit	\$0.03	\$0.03
Module Grounding	\$0.01	\$0.00
Total Installed Cost (\$/W)	\$0.72	\$0.85
Optimizer Boost	0%	0%
Specific Production (kWh/kWp/year)	1545	1900
PPA Rate	0.089	0.09
Investment Tax Credit	0%	0%
Discount Rate	14%	14%
Productive years	25	30
Degradation	0.70%	0.50%
Operations cost	0.70%	0.40%
Bi-Facial Boost	n.a.	15%
Total Lifetime Energy Produced (kWh)	172,408,335	258,611,059
Total Lifetime Cost	\$3,747,401	\$4,382,494
Calculated LCOE (\$/kWh)	\$0.02174	\$0.01695
Calculated LCOE (¢/kWh)	2.174	1.695
Total Lifetime Revenue	\$15,344,342	\$23,016,384
IRR	17%	18%
Capex	\$3,575,387	\$4,263,083
NPV	\$566,226	\$977,944
ROI Years	5.7	5.3
		22%

LIST OF ACRONYMS

Term	Definition
2 sigma	In Statistics stands for two standard deviations away from the mean in a normal distribution
AC	alternating current
BOS	Balance of System
Cu	copper
EPIC	Electric Program Investment Charge
kWh	kilowatt per hour
µm	micrometer
MW	megawatt
PV	photovoltaic
SolarMAT	Solar Manufacturing Technology
Si	silicon
W	watt
Wp	per wafer
WPH	wafer per hour