CALIFORNIA ENERGY COMMISSION

CALIFORNIA NATURAL RESOURCES AGENCY

ENERGY RESEARCH AND DEVELOPMENT DIVISION

FINAL PROJECT REPORT

Low-Cost, High-Reliability Thermoelectrics for Waste Heat Conversion

May 2024 | CEC-500-2024-039

PREPARED BY:

PI – Dr. Ravi Prasher
Co-PI – Dr. Vi Rapp
Dr. Yuqiang Zeng
Lawrence Berkeley National Laboratory
Primary Authors

Chuck Gentry
Project Manager
California Energy Commission

Agreement Number: EPC-16-042

Kevin Uy
Branch Manager
ENERGY SUPPLY BRANCH

Jonah Steinbuck, Ph.D.
Director
ENERGY RESEARCH AND DEVELOPMENT DIVISION

Drew Bohan
Executive Director

ACKNOWLEDGEMENTS

The work described in this report was conducted at the Lawrence Berkeley National Laboratory Combustion Laboratory and funded by the California Energy Commission's Electric Program Investment Charge (EPIC) program, under contract EPC-16-042. Lawrence Berkeley National Laboratory is supported by the United States Department of Energy under contract number DE-AC02-05CH11231. The research team thanks Lin Yang, Sumanjeet Kaur, and Buyi Zhang at LBNL for their contributions to the thermoelectric characterization. The team acknowledges the fabrication work led by Professor Xiaolin Zheng and her group at Stanford including Rui Ning, Daihong Huh, Yunzhi Liu, Yue Jiang, Jihyun Beak, and Juyoung Leem.

PREFACE

The California Energy Commission's (CEC) Energy Research and Development Division supports energy research and development programs to spur innovation in energy efficiency, renewable energy and advanced clean generation, energy-related environmental protection, energy transmission, and distribution and transportation.

In 2012, the Electric Program Investment Charge (EPIC) was established by the California Public Utilities Commission to fund public investments in research to create and advance new energy solutions, foster regional innovation, and bring ideas from the lab to the marketplace. The EPIC Program is funded by California utility customers under the auspices of the California Public Utilities Commission. The CEC and the state's three largest investor-owned utilities—Pacific Gas and Electric Company, San Diego Gas and Electric Company, and Southern California Edison Company—were selected to administer the EPIC funds and advance novel technologies, tools, and strategies that provide benefits to their electric ratepayers.

The CEC is committed to ensuring public participation in its research and development programs that promote greater reliability, lower costs, and increase safety for the California electric ratepayer and include:

- Providing societal benefits.
- Reducing greenhouse gas emission in the electricity sector at the lowest possible cost.
- Supporting California's loading order to meet energy needs first with energy efficiency and demand response, next with renewable energy (distributed generation and utility scale), and finally with clean, conventional electricity supply.
- Supporting low-emission vehicles and transportation.
- Providing economic development.
- Using ratepayer funds efficiently.

For more information about the Energy Research and Development Division, please visit the CEC's research website (www.energy.ca.gov/research/) or contact the Energy Research and Development Division at ERDD@energy.ca.gov.

ABSTRACT

Thermoelectrics operating at high temperatures can cost-effectively convert waste heat and compete with other zero-carbon technologies. Among different high-temperature thermoelectric materials, silicon nanowires possess the combined attributes of cost effectiveness and mature manufacturing infrastructure. Despite significant breakthroughs in silicon nanowire-based thermoelectrics for waste heat conversion, the efficiency and operating temperature has remained low. This research project reports on the synthesis of large-area, wafer-scale arrays of porous silicon nanowires with ultra-thin silicon crystallite size of about 4 nanometers. Measurements show much higher efficiency than bulk silicon and higher efficiency than any nanostructured silicon-based thermoelectrics reported in the literature at 801°F (427°C). Towards device-level applications, the research team fabricated high-quality double-sided silicon nanowire arrays, with significantly improved performance. Therefore, this project demonstrates the potential of silicon nanowires for high-temperature waste heat recovery.

Keywords: silicon, nanowires, SiNW, thermoelectrics, high temperature, waste heat

Please use the following citation for this report:

Prasher, Ravi, Vi Rapp, Yuqiang Zeng. 2024. *Low-Cost, High-Reliability Thermoelectrics for Waste Heat Conversion.* California Energy Commission. Publication Number: CEC-500-2024-039.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Executive Summary

Lawrence Berkeley National Laboratory and Stanford University developed a novel and cost-effective process for creating advanced thermoelectric materials constructed from silicon nanowire arrays. This process demonstrated, with a prototype device, both its performance and ability to scale to mass production for heat-to-electricity conversion using waste heat from the industrial sector that is available at high-temperature waste streams. This project will lead to technological advancements that will help the state of California overcome barriers to achieving its statutory energy mandates. Specifically, it will help provide low-cost, reliable, affordable, and mass-producible waste-heat recovery technology that can convert high-temperature waste heat at both production and retail electricity levels in California.

Background

Industrial facilities such as refineries, cement plants, and oil and gas operations have over 763 megawatts of electricity-generating potential from waste heat in California. Most of the potential waste heat from the industrial sector is available from high-temperature waste streams. Thermoelectrics, or materials that create electricity from temperature differences, are one of the most prominent technologies available for harvesting waste heat and converting it to useful energy without generating greenhouse gas emissions. Unfortunately, state-of-the-art thermoelectrics are only capable of operating at lower temperatures (less than 572 degrees Fahrenheit [°F] or 300 degrees Celsius [°C]) with very low efficiency (4 to 5 percent) when converting heat to electricity. The development of silicon nanowire-based thermoelectric module devices that can operate at high temperatures could potentially enable low-cost energy conversion efficiencies greater than 10 percent.

Project Purpose and Approach

This project aimed to develop a novel and cost-effective process for creating advanced thermoelectric materials constructed from silicon nanowire arrays, and to demonstrate, with a prototype device, its performance and ability to scale to mass production for heat-to-electricity conversion. Constructing thermoelectric materials from silicon nanowire arrays increases operating temperature (up to 1521°F [827°C]) and increases heat-to-electricity conversion efficiency to at least 10 percent (about 2.5 times higher than current market thermoelectrics). Additionally, implementing silicon nanowire arrays will enable the production of cost-effective waste heat recovery systems capable of penetrating the energy recovery market in a large variety of California industries, including petroleum refining and cement plants, and enabling access to multi-billion-dollar global markets. This project encompassed all aspects of developing silicon nanowire thermoelectric materials, from materials synthesis through advanced characterization; thereby, demonstrating the technical and economic advantages of the device while advancing the applied research of nanowire technology.

The goals of this Agreement were to:

1. Develop a cost-effective mid- to high-temperature range (752°F [400°C] to 1472°F [800°C]) p-type thermoelectric material and waste heat recovery technology.
2. Reduce electricity-related carbon emissions.
3. Improve remote power generation technology.
4. Advance nanowire-based nanotechnology.

The objectives of this Agreement were to:

1. Demonstrate an etch process on at least four silicon wafers that produce nanowire arrays with diameters less than 400 nanometer and length greater than 400 micrometer.
2. Demonstrate at least one boron doped silicon nanowire array with doping level greater than $1x10^{19}$ atoms/centimeter^{-3}. (Centimeter^{-3} represents cubic centimeters per cubic centimeter, which is a unit of density.)
3. Demonstrate at least one free standing, filled array of silicon nanowires with areal density greater than 30 percent.
4. Demonstrate at least one metallized silicon nanowire array sample with electrical continuity through the array.
5. Demonstrate at least one silicon nanowire device prototype and laboratory measurements of resistivity, Seebeck coefficient (voltage per unit temperature difference), and power from room temperature to 1112°F (600°C).

Key Results

Techno-economic Model

The project team developed a techno-economic model for waste heat conversion technologies. The model enables researchers to better predict the sectors and conditions that will be ideal for waste heat conversion. Analysis under optimistic assumptions showed that waste heat conversion is only economical above 302°F (150°C) with power output in the range of 100 kilowatt to 1 megawatt. This is important for prioritizing research and development for waste heat conversion technologies.

Silicon Nanowire Template, Etch, and Doping Optimization

The research team synthesized uniform porous silicon nanowires with ultra-thin silicon crystallite (size 3.8 to 4.7 nanometers) by combining nanoimprint lithography with top-down metal-assisted chemical etching method. The prepared silicon nanowires from silicon wafers have diameters about 200 nanometers and lengths of over 400 micrometers, as specified by the first objective listed above. The research team also determined the doping concentration of various silicon nanowires tested, which was an advancement that had not been accomplished in previous work. This allowed the team to systematically vary doping concentration and porosity to optimize the figure of merit. The figure of merit is a measurement calculated to evaluate the efficiency of a thermoelectric material at a given temperature. To achieve high

electrical conductivity for the porous silicon nanowires, a post-doping process was conducted. A boron doping level of $p=2.2\times10^{20}$ atoms/centimeter^{-3} was achieved followed by the post-doping process, meeting the second objective listed above.

Thermoelectric Measurements of Single Silicon Nanowires

The research team used a house-built sharp microprobe to pick up an individual nanowire and place it between the gap of two side-by-side suspended membranes. Several strategies were applied to solve the technical challenges for high-temperature thermoelectric measurements. Concurrent measurements of thermal conductivity, electrical conductivity, and Seebeck coefficient (voltage per unit temperature difference) on the same nanowire show a figure of merit of 0.71 at 801°F (427°C), which is more than 18 times higher than bulk silicon. This figure of merit value is more than two times higher than any nanostructured silicon-based thermoelectrics reported in the literature at 801°F (427°C). A thermoelectric model was developed based on data collected. The model and data show that the figure of merit varies linearly with temperature leading to the conclusion that the figure of merit at 1112°F (600°C) would be about 0.873.

Free-standing Silicon Nanowires Fill and Metallization

The research team fabricated free-standing silicon nanowire arrays with ohmic contacts on both array surfaces for relevant thermoelectric properties. (Ohmic contacts are non-rectifying electrical junctions with low resistance.) Several strategies were applied to prepare the high-quality arrays and improve the electrical contact:

1. Increasing the exposed nanowire tip surface area via depositing silicon dioxide caps around the tips of silicon nanowires to hinder them from collecting in a mass or a heaping together.
2. Designing effective ohmic contacts by forming nickel-silicon alloy
3. Post doping the arrays to improve the electrical conductivity

Further, the research team developed double-sided silicon nanowire arrays with silicon nanowires of approximately 200 micrometers length on each side, with a minimized bulk silicon portion in between. This significantly improves the effective figure of merit of silicon nanowire arrays as the silicon nanowire length in previous studies was less than 100 micrometers. A free-standing silicon nanowire array filled with silicon dioxide was achieved with an areal density of 15 percent, partially meeting the third objective above with a lower areal ratio. This was limited by the lithography tool for patterning silicon nanowire available on campus. With a better lithography tool, the methodology developed can be translated to fabricate denser silicon nanowires. The wires can achieve a diameter of about 218 nanometers and a combined length of 422 micrometers with the two-sided structure.

Silicon Nanowire Array Property Characterization

The research team developed a measurement setup for thermoelectric characterization of silicon nanowire arrays, explained the difference between the thermoelectric properties of single nanowires and silicon nanowire arrays, and optimized the fabrication process and the

thermoelectric performance based on the measurement results. The electrical continuity was achieved with the silicon nanowire array, proven by the ohmic contact formation on both sides of the silicon nanowire array, meeting the fourth objective above. Through multiple fabrication-characterization-optimization rounds, the thermoelectric performance of silicon nanowire arrays was significantly improved, reaching a figure of merit of 0.24 at 801°F (427°C). As a comparison, this value reaches about 70 percent of the theoretical figure of merit of array samples assuming zero electrical contact resistance in the array. Therefore, this project demonstrates the potential of silicon nanowire for high-temperature waste heat recovery.

Silicon Nanowire-based Device Optimization and Fabrication

The research team fabricated a prototype silicon nanowire array-based thermoelectric device with paired p-type silicon nanowire legs and commercial magnesium silicide legs. Then the team evaluated the thermoelectric performance of the prototype device at different temperatures, including the voltage generation and power output. The maximal power output of the thermoelectric device exceeds 0.4 milliwatts when the temperature difference is 212°F (100°C). For a common commercial bismuth telluride-based thermoelectric generator operating under similar conditions, the electrical power output is on the order of 0.1 milliwatt, four times lower than the power generation from the thermoelectric device developed for this project. Further, the maximal power output increases significantly as the temperature difference increases, reaching above 30 milliwatts with a hot side temperature of 801°F (427°C). The research team anticipates that this value can increase proportionally as more devices are connected in series. For example, watt-level power output can be expected with about 30 devices connected.

Knowledge Transfer and Next Steps

To widely disseminate the project findings, the research team published two high impact archival journal papers (https://doi.org/10.1016/j.joule.2021.10.014 and https://doi.org/10.1038/s41467-021-24208-3) and released summaries of project successes on the team website (https://eta.lbl.gov/news/new-techno-economic-model-optimizes and https://eta.lbl.gov/news/efficient-high-temperature). To support widespread adoption of this technology, future research should focus on creating highly cost-effective silicon nanowire-based thermoelectric energy conversion systems incorporating other factors such as integration, processing, and heat exchanger costs. This project provides a promising approach for the development of high-performance thermoelectric devices using silicon nanowire arrays and opens up new opportunities for practical applications in the field of energy harvesting and waste heat recovery.

CHAPTER 1: Introduction

Roughly 50 percent of primary energy worldwide is rejected as waste heat, over a wide range of temperatures. Waste heat above 573 kelvin (K) has the highest Carnot potential (>50 percent) to be converted to electricity due to higher Carnot efficiency (Forman et al. 2016). Techno-economic analysis (Leblanc et al 2014) shows that thermoelectrics (TE) operating above 573 K can cost-effectively convert waste heat and compete with other zero carbon and waste heat conversion technologies. However, commercial deployment of high temperature TE is still elusive due to many challenges such as manufacturing scalability, reliability, chemical stability, and toxicity (Elsheikh et al. 2014). Among different high-temperature TE materials proposed (Poudel et al 2008; Heremans et al. 2008; Zhao et al. 2014; Biswas et al. 2012), silicon nanowires (SiNWs) (Hochbaum et al. 2012; Boukai et al. 2008) possess attributes that solve these challenges.

Historically, silicon (Si) was not considered for TE applications due to its very low figure of merit $(ZT) = S^2\sigma T/\kappa$ (≈ 0.01 at 300 K) caused by the high K (145 watts per meter-kelvin [W/m-K]). This changed in 2008 when researchers reported that SiNW with rough surfaces or thin SiNW arrays could achieve a low κ of about 1 W/m-K, which translated into a ZT value of about 0.6 (Hochbaum et al. 2008) and 0.24 (Boukai et al. 2008) at 300 K, respectively. To increase the energy conversion efficiency (h) of a TE module, it is important to increase both the hot side temperature (T_H) and ZT as $\eta = \left(1 - \frac{T_C}{T_H}\right) \times \frac{\sqrt{1+ZT}-1}{\sqrt{1+ZT}+T_C/T_H}$ (T_C is cold-side temperature). TE material costs also become competitive with other zero carbon energy technologies when operating temperatures exceed 550 K. T_H in many industrial waste heat sources is higher than 550 K. Increasing T_H also has a significant impact on reducing the cost of heat exchangers.

Single SiNW measurement (Hochbaum et al. 2008) for high ZT have thus far only been performed for $T_H \leq 300\ K$ due to many challenges related to high temperatures (Lee et al. 2016; Wang et al. 2018). Some of these challenges are:

1. Measurement errors at higher temperatures due to enhanced radiation heat loss to the local ambient and coupling between the heating and sensing membranes.
2. Non-stable platinum (Pt) heater/thermometer electrical resistance at high temperature.
3. Difficulty in simultaneously measuring k, S and σ on the same sample.

In previous SiNW measurements, S and σ were measured on different samples with presumably similar dimensions and sample qualities (Hochbaum et al. 2008; Diez et al. 2020). Previous measurements on SiNW were also performed on a single sample under given preparation conditions, but without a systematic study on the effects of various parameters such as doping levels (Hochbaum et al. 2008; Boukai et al. 2008; Diez et al. 2020).

Fabricating high-quality SiNW arrays with high *ZT* is challenging. In the literature, the *ZT* of arrays or devices based on SiNW is typically much lower than that of single SiNW. The following are reasons for the large deviation: the difficulty of fabricating large-area uniform SiNW arrays, the decreased contact area and poor electrical contacts associated with the agglomeration of SiNW tips, and the loss of dopants during long-time chemical etch and reduced electrical conductivity. In addition, the length of SiNW in previous studies is limited to less than 100 μm (micrometers), which largely reduces the effective *ZT* at array or device levels.

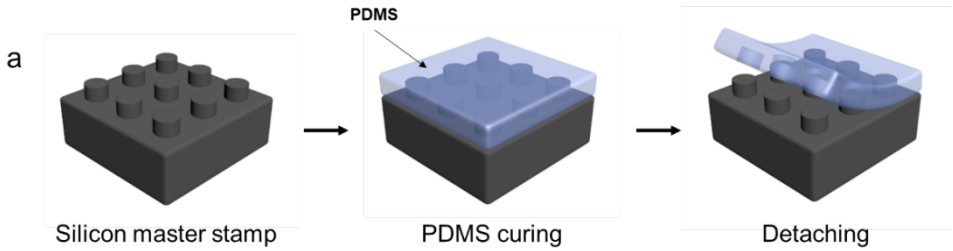
This project developed a novel and cost-effective process for creating advanced thermoelectric materials constructed from silicon nanowire arrays and which demonstrated, with a prototype device, both its performance and ability to scale to mass production for heat-to-electricity conversion. Concurrent measurements of thermal conductivity (κ), electrical conductivity (σ), and Seebeck coefficient (S) on the same nanowire show a *ZT* of 0.71 at 700 K, which is more than 18 times higher than bulk Si. This *ZT* value is more than two times higher than any nanostructured Si-based thermoelectrics reported in the literature at 700 K. Further, the research team fabricated high-quality SiNW arrays and improved their thermoelectric performance. The research team measured an array-level *ZT* of 0.24 at 700 K, which is about 70 percent of the theoretical *ZT* assuming zero electrical contact resistance in the arrays. Constructing TE materials from SiNW arrays increases operating temperatures (near and above 700 K) and allows them to be implemented where the heat-to-electricity conversion efficiency is high. Additionally, implementing SiNW will create a cost-effective TE waste heat recovery system capable of achieving an improved heat-to-electricity conversion efficiency. These improvements will attract a large variety of California industries, including petroleum refining, geothermal power, maritime and automotive, and enable access to multi-billion dollar global markets.

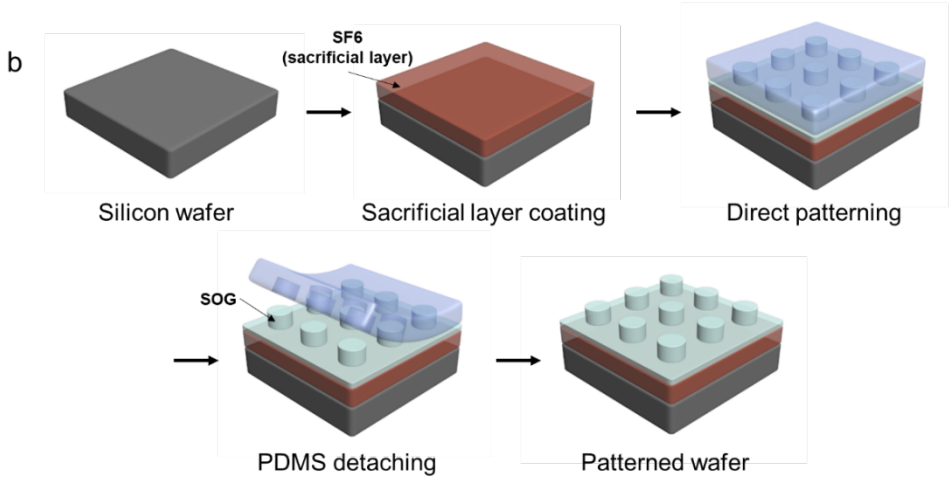
CHAPTER 2:
Project Approach

SiNW Template, Etch, and Doping Optimization

The fabrication steps to create porous SiNWs are described in Figure 1 and Figure 2. The metal pattern required for metal-assisted chemical etching (MACE) was formed using direct patterning and lift-off methods, and conventional MACE was conducted using the metal catalyst patterned on a silicon wafer. To do this, the poly-dimethylsiloxane (PDMS) mold was first duplicated from the square arrayed pillar type silicon master stamp which has a diameter of 300 nanometer (nm) and a period of 600 nm (Figure 1a). SYLGARD 184 (Dow) A and B were mixed with an 8:1 ratio and poured onto the pre-treated hydrophobic silicon master stamp. The solid PDMS mold was detached after baking for four hours at 248 degrees Fahrenheit (°F) (120 degrees Celsius [°C]) on the hot plate with the reverse structure of the silicon master stamp (Extended Data Figure 3a). Sulfur hexafluoride (SF6) (MICROCHEM, USA), which is used as a sacrificial layer, was spin-coated on the starting silicon wafer and baked for seven minutes at 338°F (170°C). Next, 4.5 weight percent (wt%) spin-on-glass (SOG) solution (250F, Filmtronics, USA) was spin-coated on the prepared PDMS mold and transferred to the SF6 coated silicon wafer (Figure 1b). To fabricate the template for metal deposition, two-step reactive-ion-etching (RIE, PlasmaPro 80, Oxford) was conducted. The SOG layer and SF6 layer were sequentially etched with trifluoromethane (CHF_3)/oxygen (O_2)/argon (Ar) and O_2/Ar under conditions of 350 watts (W), 25 millitorr (mTorr), 60 seconds (s) and 350W, 10mTorr, 90s, respectively (Figure 2a-c). Twenty nm of gold (Au) and 60 nm of silver (Ag) were then deposited on the patterned silicon wafer using e-beam evaporation (Kurt J. Lesker). After the lift-off process, the template was removed, and only the patterned metal layer was placed on the starting silicon wafer (Figure 2d-e). In the lift-off process, instead of acetone, dimethylformamide was used to prevent oxidization of the Ag layer. The metal patterned silicon wafer was immersed in a hydrofluoric acid (HF) and hydrogen peroxide (H_2O_2) mixed solution to etch silicon using the Au/Ag layer as the catalyst. The concentration of HF was fixed at 4.8 M (molarity) and the concentration of H_2O_2 was changed from 0.22 M to 0.44 M to vary porosity. After two hours etching in the solution at 77°F (25°C), porous SiNWs were fabricated with a height of 25 μm (Figure 2f). The patterned metal catalyst was removed using a nitric acid (HNO_3) and hydrochloric acid (HCl) mixed solution with a ratio of 1:3.

Figure 1: Schematic Drawing Showing the Detailed Direct-Printing Process



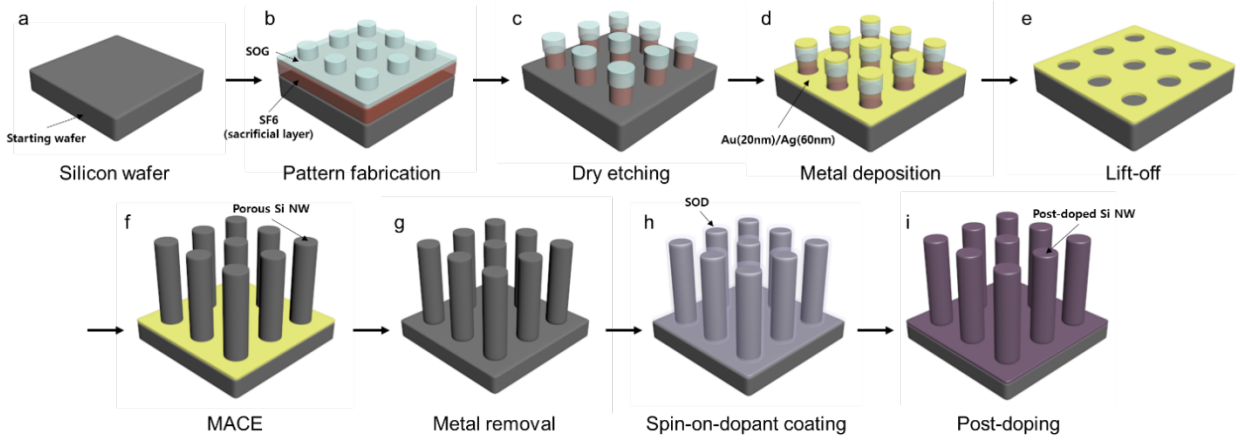


(a) Replicating the nanopatterned PDMS mold from a silicon master stamp and (b) Sacrificial layer coating and fabrication of SOG nanopattern as the template for subsequent metal deposition.

Source: Stanford University

To achieve high electrical conductivity for the porous SiNWs, a post-doping process was conducted. This technique is based on solid-state dopant diffusion and comprised of two stages: dopant pre-deposition and diffusion. First, SiNWs were dip-coated with the high concentration boron solution (SOD, 2.0 to2.5 wt% Boron in SOG solution) (Figure 2h), followed by annealing in a tube furnace (Ar 95 volume percent [vol%]/O_2 5 vol%) at 1562°F (850°C) for 30 minutes, and the coated dopant solution was then removed using 2wt% HF solution for 10 minutes (Figure 2i). Post-doped samples with higher doping levels (f = 46 percent, $p = 2.2\times10^{20}$ cm^{-3} [cubic centimeters]) were prepared by repeating the previous step using the same condition, and lightly post-doped sample (f = 46 percent, $p = 4.7\times10^{18}$ cm^{-3}) was annealed at 1292°F (700°C) for 15 minutes under the same gas condition.

Figure 2: Schematic Diagram Showing the Fabrication Process of Porous SiNWs



(a-b) Direct printing of SOG materials, (c) reactive ion etching, (d) metal deposition and (e) lift-off process to prepare metal patterned silicon wafer. (f-g) Conventional MACE was conducted to etch silicon using patterned metal as a catalyst. (h-i) post-doping was conducted using spin-on dopant (SOD) coating and subsequent annealing process.

Source: Stanford University

Individual SiNW Property Characterization

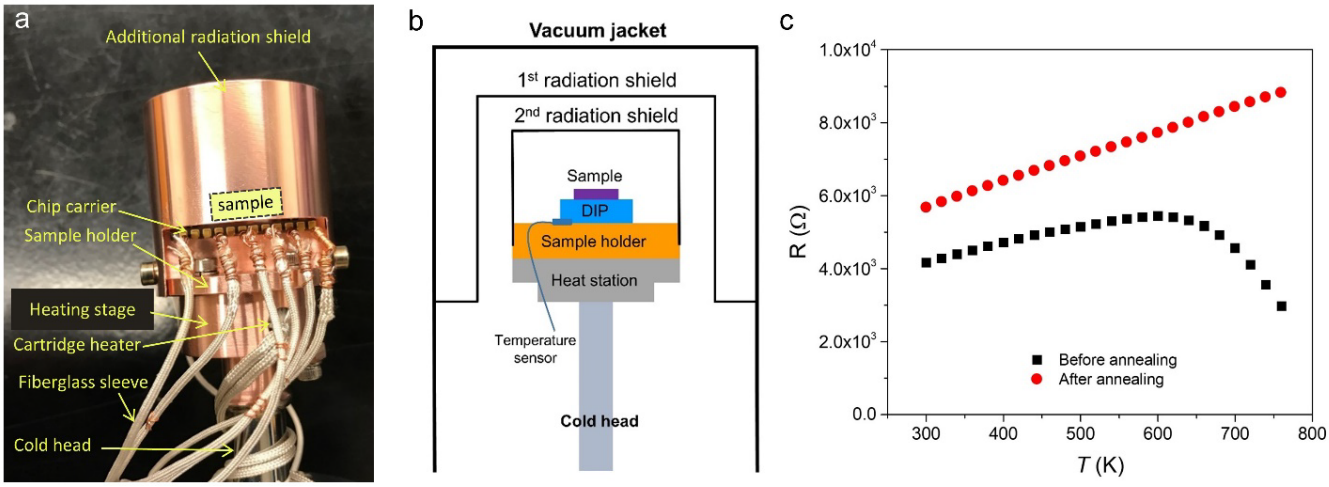
For thermoelectric properties measurements, the porous SiNW arrays were first immersed in reagent alcohol to form a suspension. After sonicating for about 10 seconds, a droplet of the suspension was drop-casted on a piece of PDMS substrate. The research team then used a house-built sharp microprobe to pick up individual nanowire and place it between the gap of two side-by-side suspended membranes. The microdevice was then loaded in a cryostat (Janis VPF-800) and the thermoelectric properties were measured under high vacuum ($<1 \times 10^{-6}$ millibar) conditions.

There are several technical challenges for high-temperature measurements, including:

1. Sample temperature deviation from the target temperature due to radiation heat loss.
2. Non-stable platinum heater/thermometer electrical resistance at high temperatures.
3. Enhanced background heat transfers due to thermal radiation between the heating and sensing membranes.

Several strategies were adopted to overcome these challenges. First, to minimize the radiation heat loss from the measurement device to the surrounding vacuum shroud, an additional radiation shield was adopted and thermally anchored on the heating stage (Figures 3a and b). The radiation shield, which was made of surface polished copper with low emissivity of 0.02, helped reach a temperature closer to the target value and reduced the settling time at each temperature point. To accurately monitor the temperature of the measurement device, a thermocouple (Type E, Lakeshore) was placed directly under the chip carrier and tightly clamped against the sample holder. Second, to increase the stability of the electrical behavior for the platinum heater/thermometer, the microdevice was annealed at 1000 K for five minutes in an argon atmosphere prior to the measurements (Figure 3c). Finally, to account for the residual thermal conductance from the background thermal radiation between the two suspended membranes, instead of using the simple estimation based on blackbody limit, the research team directly measured a blank device of identical configuration, and the background conductance was then subtracted from the measured total thermal conductance to obtain the sample intrinsic thermal conductance.

Figure 3: Measurement Technique for High-Temperature TE Properties



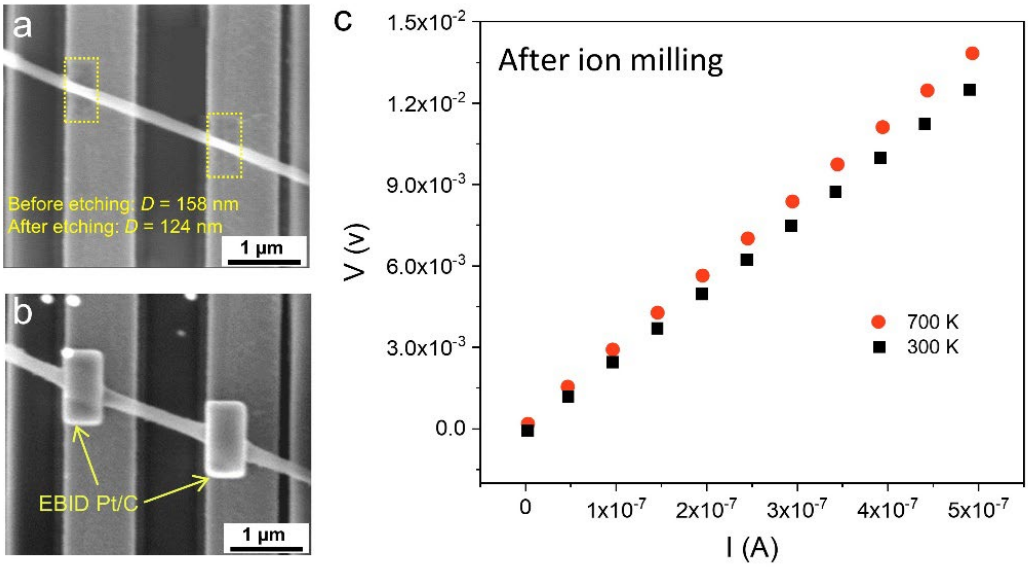
(a) Photo showing an additional radiation shield thermally anchored on the heating stage of the measurement setup to minimize the radiation heat loss from the measurement device to the surroundings. (b) Schematic drawing of (a) for a better illustration. (c) The measured electrical resistance of heating side platinum thermometer before and after the annealing treatment. It can be seen that after annealing, the measured R increases monotonically with temperature from 300 K to 760 K. Also, the measured R is reproducible in three measurements.

Source: Lawrence Berkeley National Laboratory (LBNL)

The research team measured the electrical resistance of the nanowire using the four-probe method to avoid the effects of contact electrical resistance (Figure 4). A direct current (DC) voltage output from the data acquisition board (National Instruments PCI6052e) was used as the voltage source, which was connected to a large resistor (1 megaohm [MΩ]) in series with the microdevice. During the measurements, a sweeping DC current was applied to the porous SiNW through varying the DC output voltage. The research team measured the voltage difference between the two inner electrodes of the nanowire sample using a voltage amplifier (Stanford Research Systems, SR560). Simultaneously, the DC current was measured by a current amplifier (Keithley 6487).

The research team obtained the temperature-dependent electrical resistance by fitting the measured linear I-V (current-voltage) curve. To ensure accurate measurements for samples with a large resistance (>1 MΩ), the measured voltage signal is passed through an instrumentation amplifier (Texas Instruments INA110) with a large input impedance (>10 gigaohms [GΩ]) before being fed into the voltage amplifier (SR560). To cancel out the effects of temperature fluctuation caused by the temperature controller and increase the sensitivity for thermal conductivity measurements, a Wheatstone bridge circuit was adopted by introducing a blank device at the sensing side of the measurement device. During the thermal measurements, the Seebeck coefficient for each sample was simultaneously measured by monitoring the temperature difference of the heating and sensing membranes and the induced voltage difference (SR560) across the two inner electrodes of the measurement device.

Figure 4: Ion Milling and EBID to Enable Electrical Contact



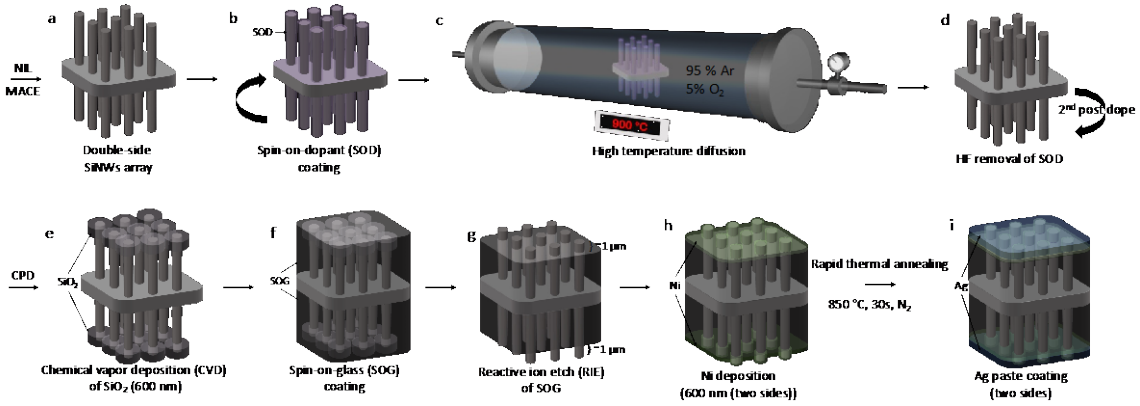
Scanning electron microscope (SEM) images of a porous SiNW (a) before and (b) after locally ion milling at the contacts between the nanowire and underlying electrodes. Electron beam induced deposition (EBID) of platinum/carbon is subsequently performed at the junctions to enable good electrical contact. (c) Measured I-V curve of the porous SiNW after ion milling and EBID deposition, where the linear I-V trend suggests ohmic contacts is established both at 300 K and 700 K.

Source: LBNL

Free-Standing SiNW Fill and Metallization

The fabrication steps of free-standing SiNW with filler and metal ohmic contacts are shown in Figure 5. The NIL (nano imprint lithography) and MACE (metal assisted chemical etch) fabricated double-sided SiNW array (Figure 5a) is composed of around 20 μm middle bulk Si and around 200 μm SiNW on both the top and bottom sides. The SiNW array was coated by spin-on-dopant (SOD) and then put in a 1652°F (900°C) tube furnace twice for the boron post-doping process like the best performance single SiNW post-doping process (Figure 5b-5d). Critical point drying was applied to the SOD removed double-sided SiNW array to avoid nanowire tip agglomeration (Figure 5e). Chemical vapor deposition (CVD) of silicon dioxide (SiO_2) around the tips of the SiNW was used to ensure the tip separation (Figure 5f). SOG (Filmtronics spin-on-glass 315F) was used as the filler material to give SiNW array mechanical support (Figure 5f). Reactive ion etching of the SOG was used to expose the SiNW tips (Figure 5g). To form ohmic contact for the SiNW array, nickel (Ni) was deposited on the exposed SiNW tips using ebeam evaporation with post deposition rapid thermal annealing (Figure 5h). Silver paste was coated on both side of the double-side SiNW array to reduce the surface roughness and enhance electrical conductivity (Figure 5i).

Figure 5: Schematic Drawing Showing the SiNW Filling and Metallization Process



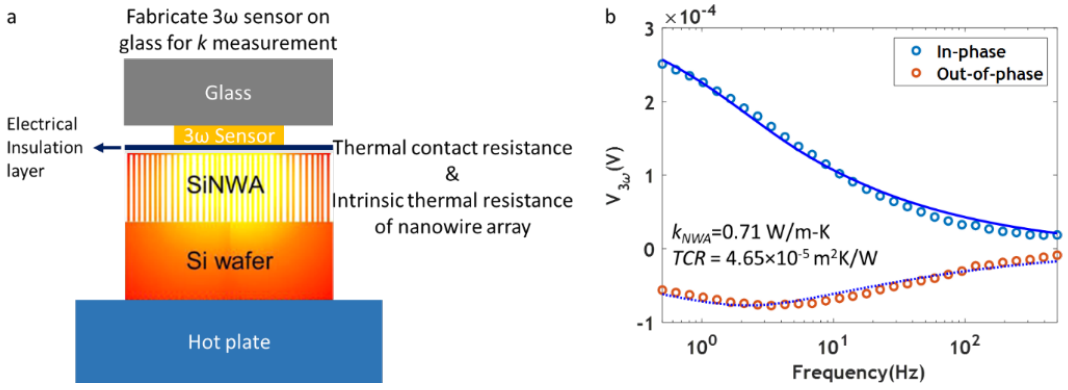
(a) double-sided SiNW array after NIL and MACE, (b-d) two times post doping of SiNW array, (e-g) SiNW array filling with SiO_2, (h-i) ohmic contact metal electrode formation on SiNW array.

Source: Stanford University

Silicon Nanowire Array Property Characterization

For TE measurement of SiNW arrays, the research team built different measurement setups for determining the conductivity (*k*), electrical conductivity (σ), and Seebeck coefficient (S). The 3ω technique (Cahill 1990; Dames & Chen 2005; Tong & Majumdar 2006; Borca-Tasciuc et al. 2001) was chosen for the thermal conductivity measurement. (See Figure 6a for the thermal sensor fabricated on glass.) The 3ω measurement allowed the research team to extract the intrinsic thermal conductivity of SiNW array by simultaneously determining both the intrinsic *k* and the thermal contact resistance between the sensor and array. This advantage originates from the capability of varying the frequency and thermal penetration depth, which enables extracting thermal properties at different locations. Figure 6b shows a representative fit to the frequency-dependent results, and the extracted room-temperature *k* (0.71 W/m-K) agrees well with the predicted *k* using single nanowire results.

Figure 6: Thermal Conductivity Measurement Using 3ω Method

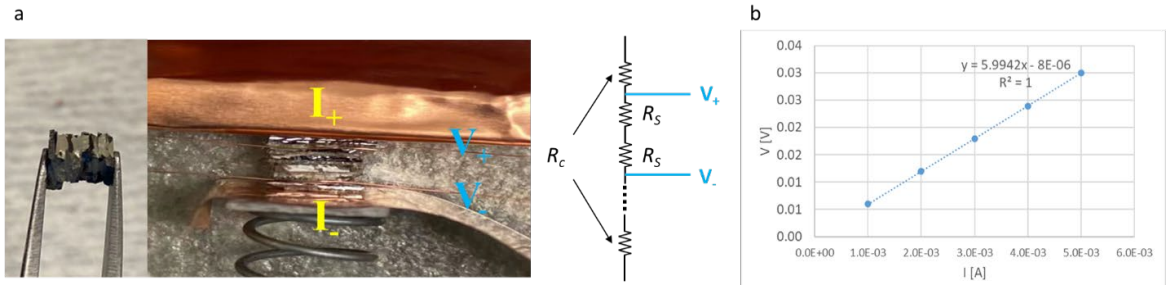


(a) Schematic of the 3ω sensor on glass for measuring the thermal conductivity. (b) Frequency-dependent thermal responses. Fitting to the full frequency range data allowed the research team to extract both the intrinsic thermal conductivity of SiNW array and the thermal contact resistance between the array and sensor.

Source: LBNL

The research team measured the electrical conductivity of SiNW arrays using the four-probe method. Two-probe measurements were typically performed for this type of measurement due to the difficulty of placing voltage probes across the thin SiNW array of about 500 µm. To overcome this challenge and avoid the effects of contact electrical resistance, the research team prepared a stack of SiNW arrays so that the voltage could be measured using additional voltage probes (Figure 7a). Silver paste was used to bond the SiNW arrays for a minimized electrical contact resistance in between. During the measurements, a range of alternating current (AC) was applied using a current source and the voltage was measured with a lock-in amplifier. Figure 7b displays the linear I-V feature of the stack, which verifies the ohmic contact in the SiNW array samples.

Figure 7: Electrical Conductivity Measurement Using the Four-Probe Technique

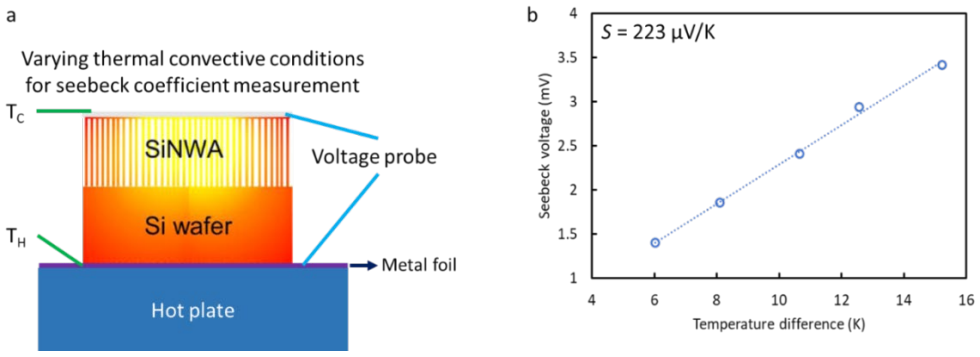


(a) Schematic of the stack of SiNW arrays used for the four-probe electrical measurement. The electrical contact effect is removed with the additional voltage probes. (b) Representative plot of voltage vs. current for determining electrical resistance.

Source: LBNL

Figure 8a shows the schematic of the setup for the measurement of Seebeck coefficient. A hot plate was used to adjust the ambient temperature. The temperature difference across the array was controlled by varying the thermal convective conditions, e.g., a high heat transfer coefficient on the array surface results in a large temperature difference. The voltage was measured using a multimeter and the Seebeck coefficient was determined by calculating the slope of voltage vs. temperature difference (Figure 8b).

Figure 8: Seebeck Coefficient Measurement of SiNW Array



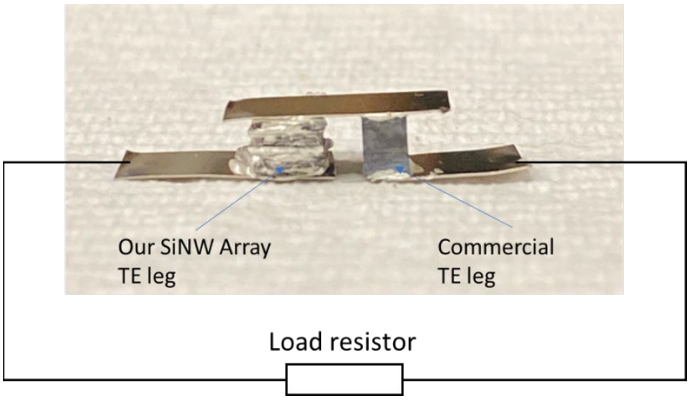
(a) Schematic of the setup used for Seebeck coefficient measurement. The temperature difference was adjusted by varying the thermal convective conditions and measured using two thermocouples. (b) Representative plot of the measured voltage vs. temperature difference for determining the Seebeck coefficient.

Source: LBNL

Silicon Nanowire Based Device Optimization and Fabrication

For the fabrication of a prototype SiNW array-based TE device with paired p-type SiNW legs and commercial magnesium silicide legs, multiple SiNW array layers (approximately 400 μm thick per layer) were bonded together using silver paste for matching the millimeter-scale commercial n-type TE leg (2.5 millimeters [mm]). The unit was baked at 302°F (150°C) for two hours to fully cure the paste and improve both the electrical and thermal contact between layers. Figure 9 shows the photo of the assembled prototype TE device. In addition to measuring the voltage generation associated with the temperature difference across the device, the research team evaluated the power output in an electrical circuit with a variable load resistor. As a temperature difference was applied across the device, a current passed through both the TE device and resistor, resulting in a corresponding voltage drop.

Figure 9: A Prototype SiNW Array-Based TE Device With Paired P-Type SiNW Legs and Commercial Magnesium Silicide Legs

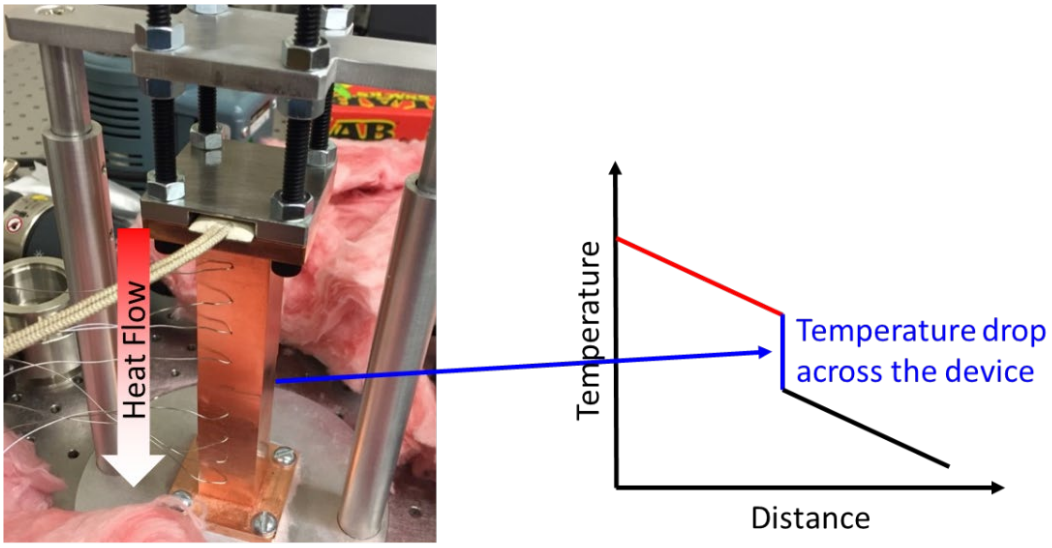


Source: LBNL

SiNW array layers are bonded together using silver paste to match the thickness of the commercial TE leg (2.5 mm). In addition to the voltage generation associated with the temperature difference, the power output was evaluated with a variable resistor.

To accurately control the temperature difference and heat flow through the device, the research team built a cut-bar apparatus (Lubner et al. 2020), shown in Figure 10. Having multiple thermal couples along the copper reference bar allowed the heat flow across the TE device to be determined using the thermal conductivity of copper, and the temperature profile along the bar. The surface temperature of the device was estimated with the measured heat flow. The heat flow and temperature difference vary as the power input changes. Accordingly, the voltage generation and power output were evaluated as a function of temperature difference and load resistance. Due to the multilayer nature of the p-type leg using the SiNW array, device-level TE performance largely depends on the electrical and thermal contact between layers. Poor electrical contact causes power consumption and reduces effective power output, while thermal contact resistance decreases temperature difference across the device (and thus the voltage generation).

Figure 10: Cut-Bar Apparatus for the TE Performance Evaluation



Source: LBNL

With multiple thermocouples along the copper reference bar, the heat flow and temperature across the TE device in between can be measured with high accuracy. The heat flow and temperature difference vary as the power input changes. Accordingly, the voltage generation and power output can be evaluated.

CHAPTER 3:
Results

The project team developed a techno-economic model for waste heat conversion technologies. The model enables researchers to better predict the sectors and conditions that will be ideal for waste heat conversion. Analysis under optimistic assumptions showed that waste heat conversion is only economical above 302°F (150°C) with power output in the range of 100 kilowatts to 1 megawatt. This is important for prioritizing research and development for waste heat conversion technologies.

SiNW Array Fabrication

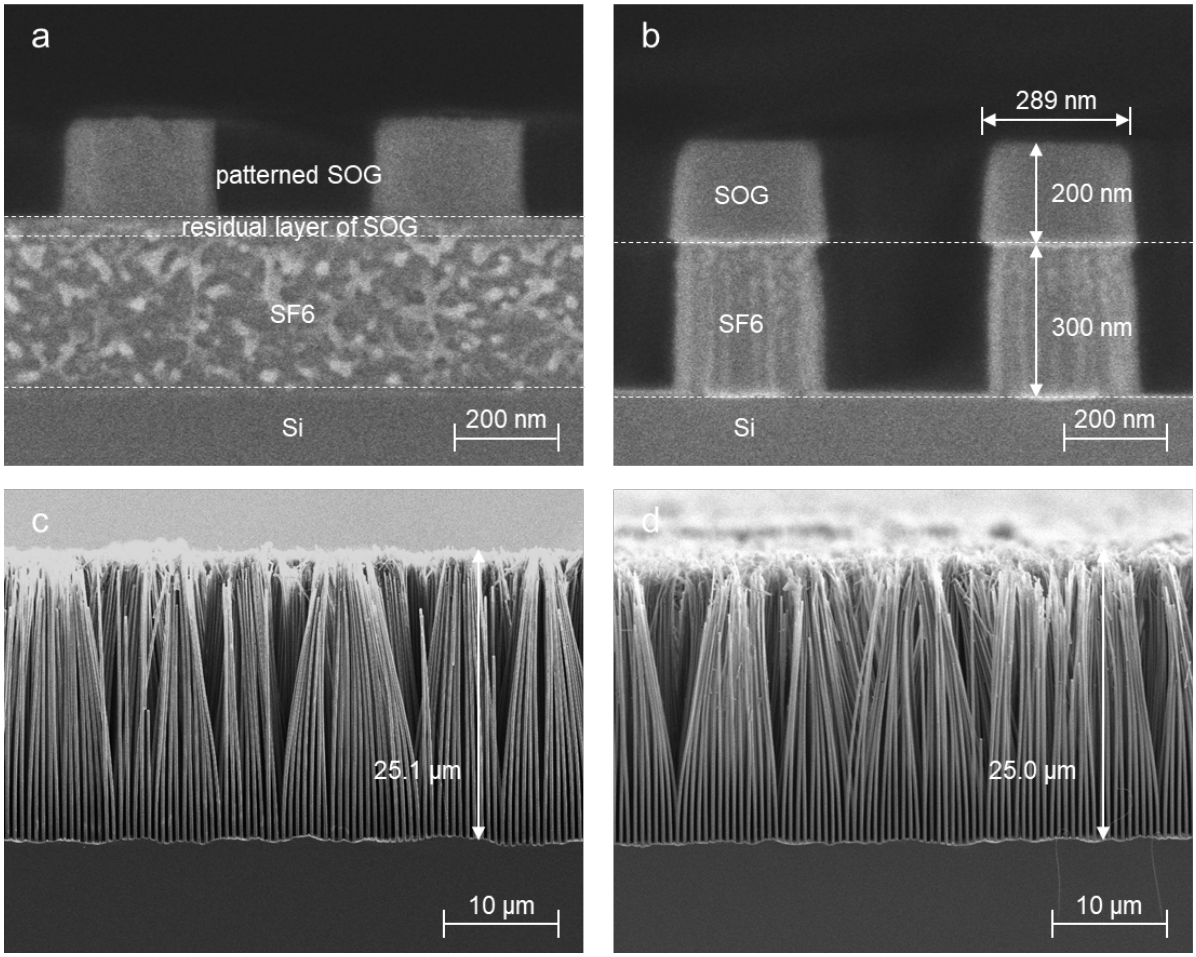
The scanning electron microscope (SEM) side view image (Figure 11a) shows the results of the direct patterning process illustrated in Figure 1b. The patterned SOG layer with cylindrical pillar pattern sits on top of the sacrificial SF6 layer along with a thin residual layer of SOG. After the dry etching process described in Figure 2c., the residual SOG layer and the sacrificial SF6 layer below the non-pillar area are removed (Figure 11b) to prepare the pattern for metal catalyst deposition. The fabricated SiNW array has around 25 μm wire length. The length was designed for the single SiNW thermoelectric measurements. The wires qualities were similar before and after the high temperature post doping process as shown in the images in Figure 11c and Figure 11d.

A project goal was to create a high aspect ratio (1000:1) SiNWs array, which requires around 300 μm length wires with 300 nm diameter. During the SiNWs metal template patterning method development, both the direct patterning method and the photo lithography method were studied. The direct patterning method was chosen over the photo lithography method because it has the advantage in the 300 nm resolution size. While the photo lithography patterns are more uniform and can do 4-inch wafer scale patterns, the method becomes unstable when the pattern size is down to 0.5 μm, so it was hard to achieve the high aspect ratio goal using the photo lithography method.

During the SiNWs MACE etching process, different H_2O_2 concentrations of the etching solution and different doping concentrations of the starting wafers were studied with respect to their influence on the final SiNWs porosity. The results are summarized in Table 1, where the fabricated SiNW porosity increases with increasing H_2O_2 concentration or starting wafer doping concentration.

The influence of the high temperature doping process on the fabricated SiNWs electrical conductivities was also studied. Table 1 shows that the wire electrical conductivity increases as the doping times and doping temperatures increase because more boron dopants were driven into the SiNWs matrix as the doping temperatures and times increased. The double doped samples were fabricated with the same high temperature annealing process mentioned in the previous section, but with two 30-minute 1562°F (850°C) annealing steps.

Figure 11: Scanning Electron Microscope Images



(a) Patterned SOG layer on the substrate, (b) Side-view after RIE, (c) Fabricated SiNW arrays after MACE, and (d) SiNW arrays after post-doping

Source: Stanford University

Table 1: Summary of Various Porous Sinw and Doping Levels Investigated in This Project

Starting wafer (p, σ, κ)	**P (~9×10^{14} cm^{-3}, 10 S/m, 145 W/m-K)[a]**		**P+ (~8×10^{16} cm^{-3}, ~10^3 S/m, 134 W/m-K)[a]**						**P++ (~1×10^{19} cm^{-3}, 10^5 S/m, 113 W/m-K)[a]**
H_2O_2 (M)	0.22		0.22				0.33	0.44	0.22
Porosity (%)	9		46				60	67	61
Post-doping	no	yes	no	yes	yes	yes	yes	yes	no
Final doping level (p, $\times10^{18}$ cm^{-3})	1.6E-5*	2.1	3.9E-3*	4.7	23	220	12.7	42	4.8

Starting wafer (p, σ, κ)	P (~9×10^{14} cm^{-3}, 10 S/m, 145 W/m-K)[a]		P+ (~8×10^{16} cm^{-3}, ~10^3 S/m, 134 W/m-K)[a]						P++ (~1×10^{19} cm^{-3}, 10^5 S/m, 113 W/m-K)[a]
Si crystallite size (nm)	4.7	4.7	3.9	3.9	3.9	3.9	3.8	3.8	3.8
κ (W/m-K)[b]	9.32	9.13	5.43	4.41	4.08	4.85	3.19	2.18	2.56
σ (S/m)[b]	0.03	3258	1.05	2886	11950	115101	32.3	0.51	3.63
S (μV/K)[b]		445.1		430.9	381.7	206.2	419.3		
ZT (300 K)		0.021		0.037	0.13	0.31	0.00053		
ZT (700 K)		0.098		0.16	0.35	0.71	0.0076		

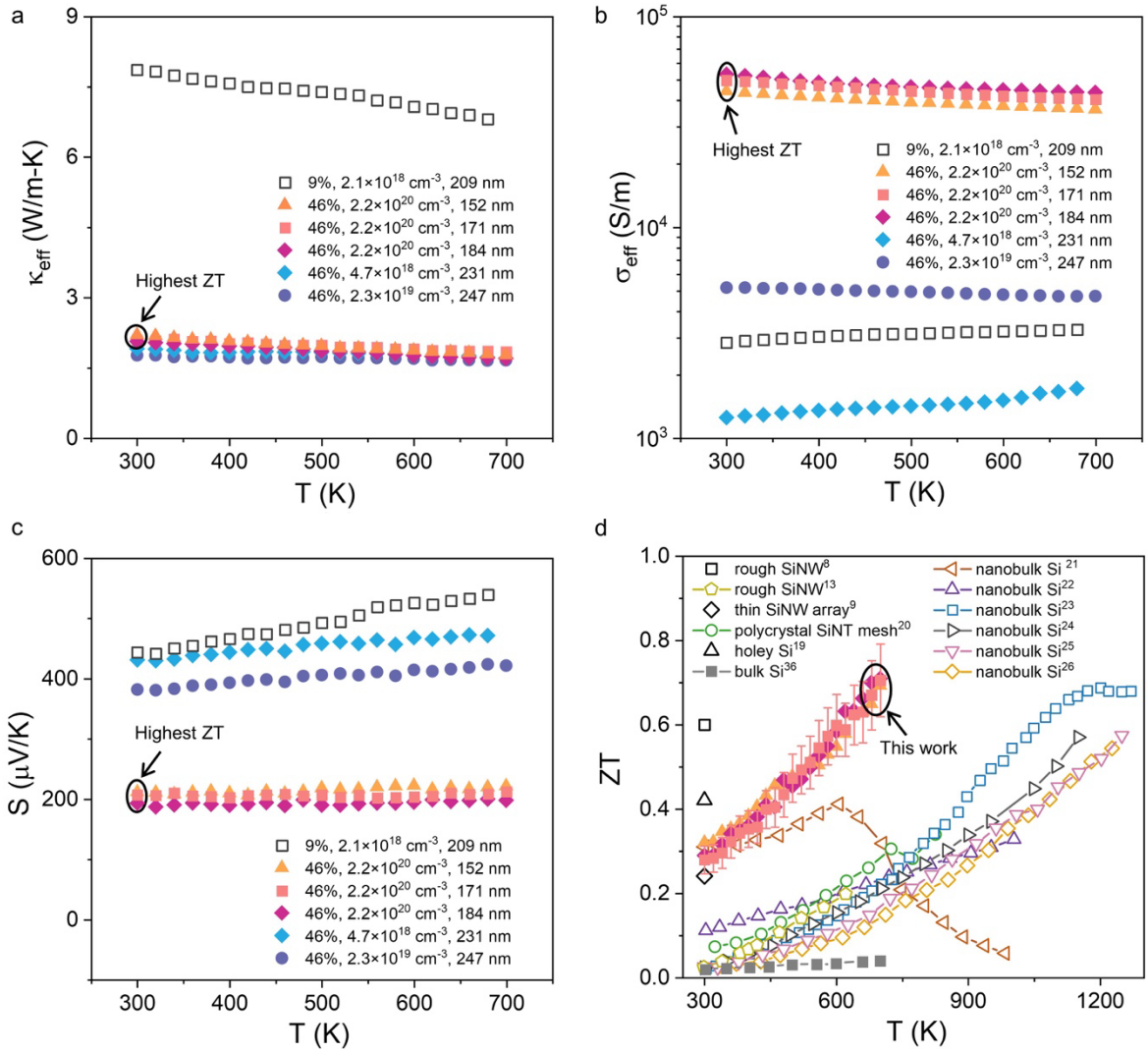
Source: LBNL

Thermoelectric Properties of Single SiNWs

Measured Room Temperature Thermoelectric Properties

The research team varied the SiNW porosity and doping concentration by changing the initial p-type Si wafer doping concentration, H_2O_2 concentration in MACE, and post doping conditions, to study their effects on the TE properties of SiNWs. Table 1 summarizes the physical properties and measured TE properties of all tested SiNWs. The porosity for SiNWs fabricated, from P, P+, and P++ wafers with 0.22 M H_2O_2, is 9 percent, 46 percent, and 61 percent, respectively (see Table 1). Higher initial Si wafer doping concentration leads to SiNWs with a higher porosity because the dopant atom sites act as preferential locations for pore formation (Weisse et al. 2012). Both κ and σ were extracted using the effective medium theory to account for the porosity (Tang et al. 2010). Although high porosity reduces κ by one order of magnitude compared to bulk Si due to pore boundary scattering, it significantly reduces σ by orders of magnitude compared to the starting wafer because of the removal of dopant atoms. Moreover, when the porosity reaches the percolation threshold (about 57 percent), electron hopping becomes the dominant mechanism for charge carrier transport (Aroutiounian & Ghulinyan 2003), and the hopping mobility could be five orders of magnitudes lower than the charge mobility of bulk Si (Aroutiounian & Ghulinyan 2003; Weisse 2013). This explains the observed ultralow σ of SiNW with high porosity. The results in Table 1 indicate that the optimization process of TE properties of SiNWs is a delicate tradeoff between porosity and doping concentration.

Figure 12: Temperature-Dependent Thermoelectric Properties



Measured (a) effective thermal conductivity, κ_{eff}, (b) effective electrical conductivity, σ_{eff}, and (c) Seebeck coefficient, S, of various porous SiNWs as a function of temperature. For the legend, the first number represents SiNW porosity, the middle one is boron doping concentration (p) measured using secondary ion mass spectrometry (SIMS, see Methods), and the last number is SiNW diameter. Note κ_{eff} and σ_{eff} are extracted based on nanowire diameter without normalizing with porosity. (d) Calculated thermoelectric figure of merit ZT for the three samples with f = 46 percent and p = 2.2×10^{20} cm^{-3} (152 nm, 171 nm, 184 nm) with the highest ZT in this work, where the previously measured ZT results of single rough SiNW, thin SiNW array, polycrystalline Si nanotube mesh, holey Si, nanobulk Si, and bulk Si (8.1×10^{19} cm^{-3} boron-doped) are plotted for comparison. The error bars represent ZT uncertainties calculated based on measurement errors in κ, σ, and S

Source: LBNL

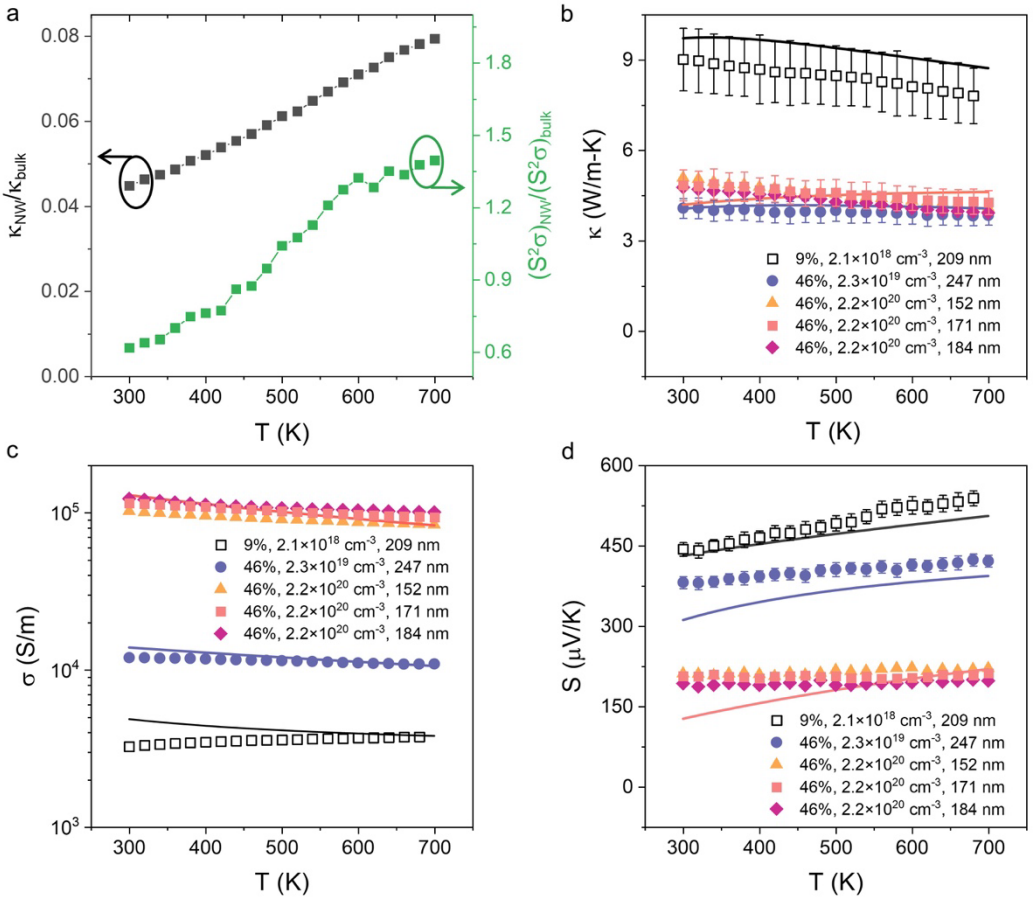
Temperature-Dependent Thermoelectric Properties

Figure 12 shows the temperature dependent κ_{eff}, σ_{eff}, and S of SiNWs of various porosity (below the percolation threshold), boron doping concentration (post-doping level), and diameter D. The values of $\kappa_{eff} = \frac{GL}{A}$ and $\sigma_{eff} = \frac{L}{RA}$ were extracted based on nanowire diameter ($A = \pi D^2/4$) without porosity correction, and G, R, and L are measured thermal conductance,

electrical resistance, and nanowire length, respectively. The effective thermal conductivity κ_{eff} (Figure 12a) is mainly affected by porosity and less sensitive to the doping concentration and diameter for the SiNWs tested here. Higher porosity leads to smaller κ_{eff} due to pore boundary scattering. The effective electrical conductivity σ_{eff} is a strong function of both the porosity and doping concentration. Higher doping concentration is needed to achieve large σ_{eff}. For similar doping concentrations, low porosity leads to large σ_{eff}. As expected, the Seebeck coefficient S shows approximately the opposite dependence as compared to σ_{eff} on doping concentration.

Among all SiNWs tested, porous SiNWs with $p = 2.2\times10^{20}$ cm^{-3} and porosity of 46 percent (152 nm, 171 nm, and 184 nm) show the highest ZT (Figure 13d). For each type of SiNW, the research team measured 3 samples and the results are consistent as shown in Figure 12d. The average ZT reaches 0.71 at 700 K. Figure 3d also shows the ZT values of Si in various forms, such as single rough SiNW (Hochbaum et al. 2008; Diez et al. 2020), SiNW arrays (Boukai et al. 2008), holey Si (Tang et al. 2010), polycrystalline Si nanotube mesh (Morata et al. 2018), nanobulk Si (Kashiwagi et al. 2019; Kessler et al. 2013; Bux et al. 2009; Zhu et al. 2016; Claudio et al. 2014; Schierning et al. 2011), and optimally doped bulk Si (Stranz et al. 2013). The ZT of the research project SiNW at 300 K lies between the ZT value obtained previously on rough SiNWs (Hochbaum et al. 2008) and thin SiNW arrays (Boukai et al. 2008). At elevated temperature, the ZT of the research project SiNW is significantly higher than other forms of Si, and only Bux et al. showed a ZT of nanobulk Si reaching 0.70 at 1100 K (Bux et al. 2009). The main reason for the higher ZT of the research project SiNWs is due to the smaller crystallite size in the research project SiNW sample (about 3.8 nm to 4.7 nm) as compared to other forms of Si where the crystalline size is at least 10 nm or higher (Kashiwagi et al. 2019; Kessler et al. 2013; Bux et al. 2009; Zhu et al. 2016; Claudio et al. 2014; Schierning et al. 2011). This leads to about a two to five times lower κ for the research project SiNW.

Figure 13: Theoretical Modeling on Thermoelectric Properties of Porous SiNWs



(a) Black square represents the ratio of porous SiNW κ (ϕ = 46 percent and p = 2.2×10^{20} cm^{-3}, 171 nm) to that of optimally doped bulk Si (8.1×10^{19} cm^{-3} boron-doped) as a function of temperature. Green squares show the ratio of power factor of porous SiNW (ϕ = 46 percent and p = 2.2×10^{20} cm^{-3}, 171 nm) to that of the optimally doped bulk Si (8.1×10^{19} cm^{-3} boron-doped). (b-d) Comparison between the measured temperature-dependent (b) κ, (c) σ, and (d) S with modeled results considering the effects of pore boundary scattering. Note that in panel (b) for the ϕ = 46 percent and p = 2.2×10^{20} cm^{-3} sample, charge carriers make a non-negligible contribution to thermal transport, and the modeled κ is the sum of the calculated lattice thermal conductivity and electronic thermal conductivity, κ_e, estimated using the Wiedemann–Franz law. The error bars in κ represent uncertainties calculated based on measurement errors in thermal conductance, porosity, nanowire length and cross-section. The error bars in σ represent uncertainties calculated based on measurement errors in electrical resistance, porosity, nanowire length and cross-section, and the magnitude of the error bars are smaller than the symbol size for σ. The error bars in S are determined as the standard deviation from linear least square fitting.

Source: LBNL

Free-Standing SiNW Fill and Metallization

Investigate a Suitable Material Capable of Filling the SiNW Array

The SEM side view image in Figure 14a shows the SiNW array after NIL and MACE. The double-sided SiNW array is mainly made of SiNW with only around 10 μm middle bulk Si, which is etched from P+ Si wafer (p=8 × 10^{16} cm^{-3}, σ=10^3 Siemens per meter (S/m), κ=134 W/m-K). Among the filler materials (such as paraffin wax, polyvinylidene fluoride, high-density polyethylene, and SOG) the research team found that the SOG material, made of SiO_2

in isopropyl alcohol solution, is the best filler material for SiNWs array due to its high-temperature sustainability.

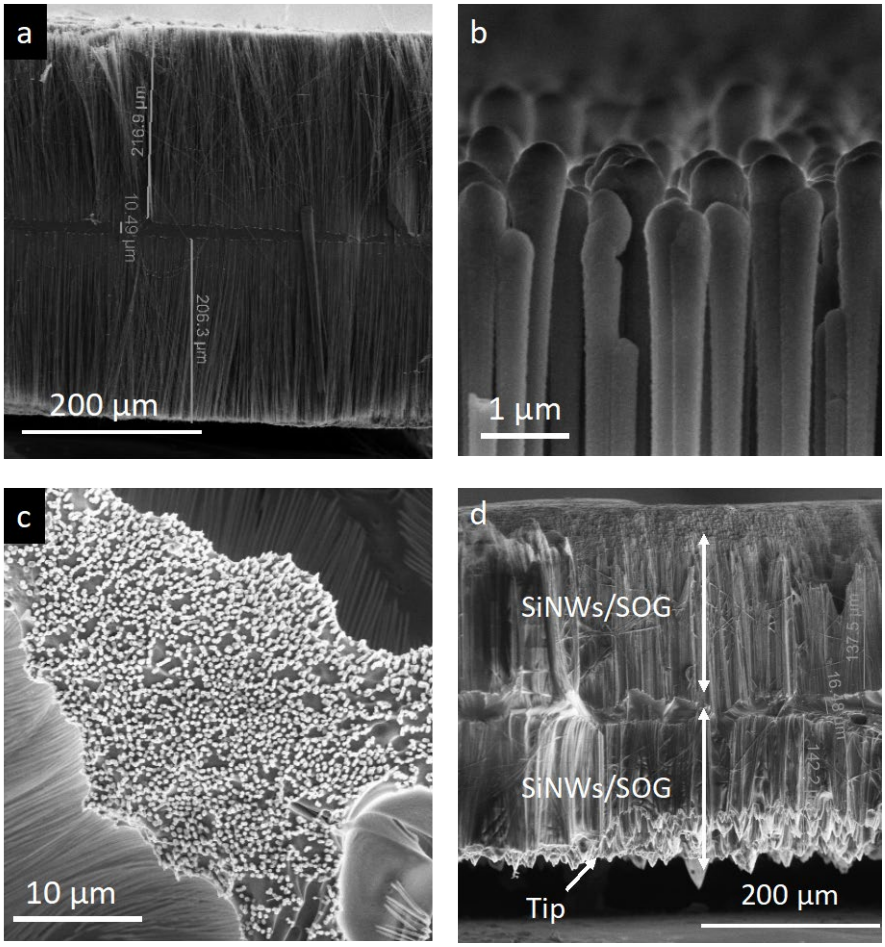
Investigate a Technique to Uniformly Expose the SiNW Tips for Metallic Contact

The research team used the CVD SiO_2 to help separate the SiNW tips for better electrical contact. The research team found that the RIE method can effectively expose the separated SiNW tips for metallization. Figure 14b shows the side view SEM image of the SiNW tips wrapped by the CVD deposited SiO_2 after the process in Figure 1e. After the SOG filling and RIE tip exposure in Figure 1f and Figure 1g, the SiNW tips are globally filling by SOG while locally separated as shown in Figure 14c, indicating the CVD SiO_2 effectively avoided the SiNW tip agglomeration.

Investigate a Front Side Metallization Layer Capable of Forming an Ohmic Contact to the Front of the SiNWs

The research team found that the Ni deposition on both the top and bottom sides of the SiNW array after rapid thermal annealing can form good ohmic contact possibly due to the formation of nickel silicide. Figure 14d shows the side view SEM of the SiNW array after the metallization process shown in Figure 1h and Figure 1i. The final SiNW length is around 300 μm combing both sides, and the middle bulk Si part is around 10 μm. The ohmic contacts of the top and the bottom sides of the SiNW array were confirmed by the linear I-V curve (Figure 15) measured on SiNW array in Figure 14d.

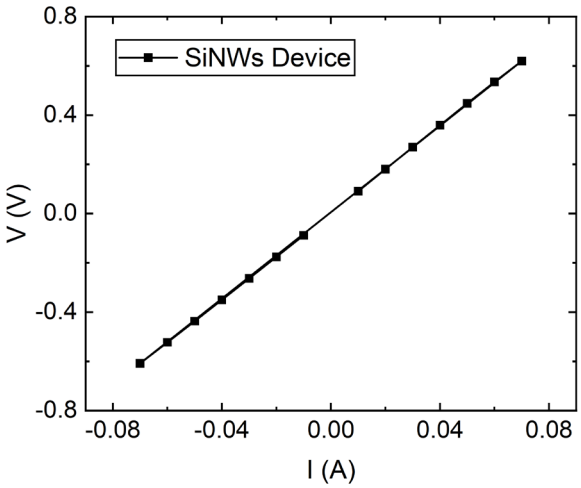
Figure 14: Scanning Electron Microscope Images



(a) side-view SiNW array after NIL and MACE, (b) side-view SiNW array tips after CVD SiO_2 deposition, (c) tilted top-view SiNW array tips after SOG filling and RIE, and (d) side-view SiNW array after metallization.

Source: Stanford University

Figure 15: I-V Scan of the SiNW Array After Metallization



Source: LBNL

Thermoelectric Properties of SiNW Arrays

Measured Room-Temperature Thermoelectric Properties

Starting from the optimal fabrication conditions for single nanowires (NWs), the research team focused on how to resolve the contact issue at the array level. The length of the NW and bulk Si part was varied by changing the etch time, which can affect the mechanical properties of NWs and thus the electrical and thermal contact. Further, the metal contact layer thickness is critical for the electrical connection. The research team studied the impact of the NW length (or the bulk Si thickness) and the Ni layer thickness on the contact and TE properties of SiNW arrays. Table 2 summarizes the layer properties and measured TE properties of all tested SiNW arrays. As the etch time increases, the bulk Si thickness reduces from 500 μm to 300 μm, 100 μm, and 20 μm, respectively. To exploit the high *ZT* of the NW, the thickness of the bulk Si part should be minimized. However, improving the electrical contact between the SiNW tip and silver paste is the key to achieving this theoretically high *ZT*. As shown in Table 1, the effective *ZT* can be as low as 0.0002 and 0.008 even with 20 μm bulk Si. Increasing the Ni layer thickness to 600 nm can largely enhance this value to 0.037. This is a result of the improved electrical connection between the exposed Si NW tips and silver paste due to the thicker metal contact layer. With the improved contact, the team noted that the poor electrical conductivity of the bulk Si becomes the bottleneck for the further optimization of *ZT*. As a comparison, the team extracted the effective TE properties of the NW portion and the *ZT* is about 0.10 at 300 K. The team identified that the good electrical contact and the high electrical conductivity of initial Si wafers are the two key factors for achieving high *ZT* at the array level.

Table 2: Measured Room-Temperature TE Properties of Sinw Arrays With Varying Ni Contact Layer Thickness and Bulk Si Thickness.

Starting wafer (p, σ, κ)	**P+ (~8×10^{16} cm^{-3}, ~100 S/m, 134 W/m-K)[a]**						
Ni layer thickness (nm)	100			200			600
Bulk Si thickness (μm)	20	70	300	20	100	300	20
σ_{eff} (S/m)[b]	11.95	25.19	59.56	464.02	36.50	67.89	1687.99
σ_{NW} (S/m)[c]	12.00	26.04	89.33	561.14	38.68	104.18	4557.46
k_{eff} (W/m-K)[b]	0.72	0.80	1.71	0.74	0.89	1.18	0.68
k_{NW} (W/m-K)[c]	0.71			0.69			0.65
S_{eff} (μV/K)[b]	212			208			223
S_{NW} (μV/K)[c]							
ZT_{eff} (300 K)[b]	0.0002	0.0004	0.0005	0.008	0.0005	0.0007	0.037
ZT_{NW} (300 K)[c]	0.0002	0.0005	0.002	0.01	0.0007	0.002	0.105

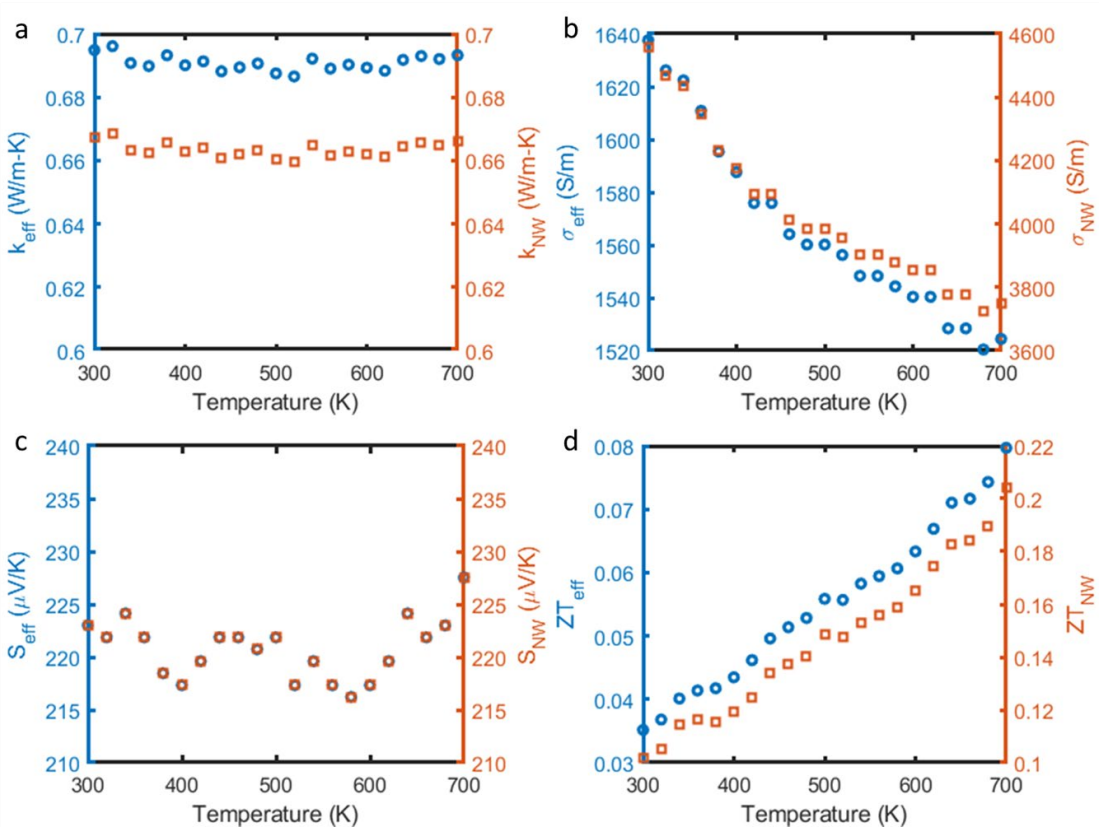
[a]: σ and κ are room temperature results adapted from Ref.[32] for bulk Si with close doping concentrations (p).
[b]: Effective properties of the SiNW arrays.
[c]: Extracted properties of the NW portion in SiNW array.

Source: LBNL

Thermoelectric Properties at High Temperatures

Figure 16 shows the temperature-dependent thermoelectric properties of the SiNW array with the highest room-temperature *ZT* (see Table 2). The weak temperature dependence of thermal conductivity, electrical conductivity, and Seebeck coefficient is similar to that of single SiNWs. In particular, the variation of k_{eff} and k_{NW} is less than 3 percent across the whole temperature range due to a balance effect, i.e., the *k* of the filler slightly increases with temperature while that of the NW decreases slightly with temperature. Since the *k*, σ, and *S* demonstrates a weak temperature dependence, the increase of *ZT* with temperature is almost linear. As shown in Figure 16d, the *ZT* of the SiNW array and NW part reaches 0.08 and 0.2, respectively. Although higher *ZT* values were reported in the literature (Kashiwagi et al. 2019; Kessler et al. 2013; Zhu et al. 2016; Claudio et al. 2014; Schierning et al. 2011; Stranz et al. 2013), it is worth noting that the electrical contact resistance was not appropriately characterized in prior works, e.g., noncontact techniques were used and/or the bulk Si part was removed for creating direct electrical connection between the NW and probes. This work provides a realistic evaluation of the electrical contact resistance in SiNW arrays which is critical for the application and optimization of TE devices.

Figure 16: Temperature-Dependent Thermoelectric Properties of SiNW Arrays



(a) Thermal conductivity, (b) electrical conductivity, (c) Seebeck coefficient, and (d) *ZT* of the SiNW array and NW portion from 300 K to 700 K. As the *k*, σ, and *S* demonstrates a weak temperature dependence, the *ZT* increases almost linearly with temperature, reaching 0.08 and about 0.2 for the array and NW part, respectively.

Source: LBNL

TE Performance of SiNW Based Devices

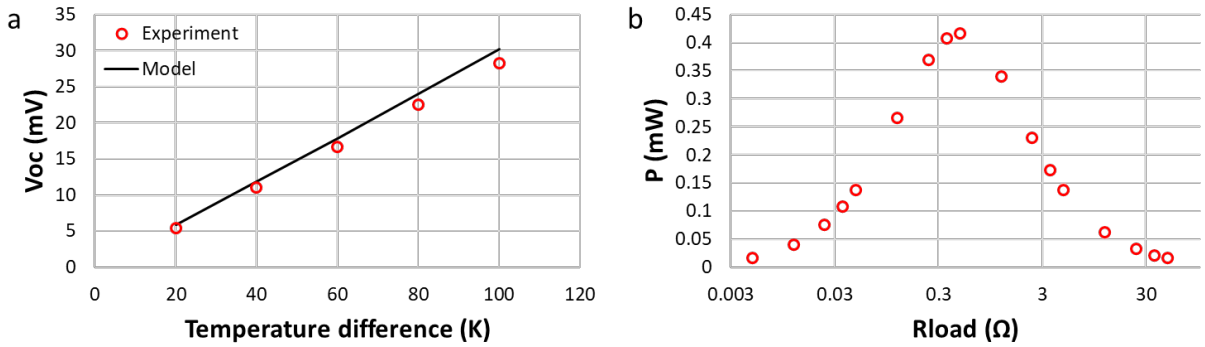
Open-Circuit Voltage and Power Output

With the optimized SiNW arrays, the research team fabricated a prototype device paired with commercial Magnesium Silicide legs. Figure 17a shows that the generated open circuit voltage increases with the temperature difference, reaching 28.3 millivolts (mV) with a temperature difference of 100 K for a single device. Assuming perfect thermal contact, the research team calculated the theoretical voltage generation using the Seebeck coefficient from previous measurements of the SiNW array. The comparison suggests that the thermal contact has a minor effect on the open-circuit voltage and confirms the high Seebeck coefficient of the research project SiNW array layers. Further, the team measured the power output as a function of load resistance. As load resistance is equal to the internal resistance of the TE device, the maximal power output exceeds 0.4 milliwatt (mW) when the temperature difference is 100 K (Figure 17b). For a common commercial bismuth telluride (BiTe)-based thermoelectric generator (Jaziri et al. 2020) operating under similar conditions, the electrical power output is on the order of 0.1 mW, four times lower than the power from the research project device. Note that these measurements are for a single device. The voltage and power can increase as more devices are connected in series for practical applications, depending on the size of the waste heat recovery system.

Power Output at High Temperatures

Previously, the research team measured the TE properties of the research project SiNW arrays from 300 K to 700 K. With the device-level TE characterization from 300 K to 400 K, the team verified the unique TE properties of the research project SiNW arrays. Further, the measured open-circuit voltage was close to the value predicted using the measured properties of the SiNW array. Thus, the device-level TE performance can be evaluated with the TE properties of each leg. Since commercial magnesium silicide (Mg2Si) TE legs were used as the n-type leg, the TE properties were well studied and provided in the literature (Kim et al. 2014). As a result, the TE performance of the project prototype device at high temperatures can be reliably evaluated with the temperature-dependent TE properties of both legs, especially the maximal power output at high temperatures. Experimentally, the team performed the measurement with temperature differences up to 100 K, limited by the heater power. A reasonable match between the model and experiment results was observed in this temperature range. As shown in Figure 18, the research teams model predicts that the maximal power output increases significantly with the temperature difference, reaching above 30 mW with the hot side temperature of 700 K. The team anticipates that this value can increase proportionally as more devices are connected in series, e.g., watt-level power output can be expected with about 30 devices connected.

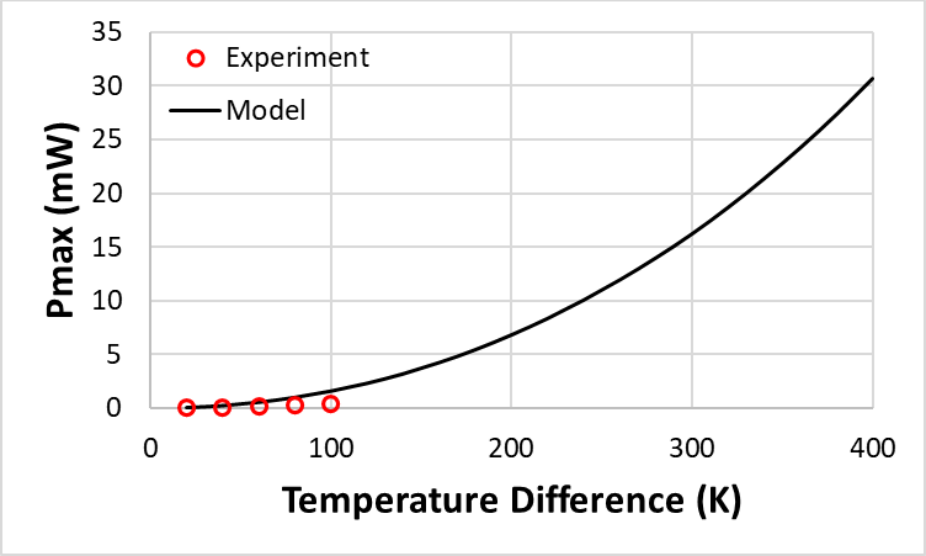
Figure 17: Open-Circuit Voltage and Power Output



(a) Increase of open-circuit voltage with the temperature difference. (b) Power output as a function of the load resistance with a temperature difference of 100 K.

Source: LBNL

Figure 18: Maximal Power Output as a Function of Temperature Difference up to 400 K



Source: LBNL

With the measured TE properties of SiNW array from 300 K to 700 K, the maximal power output can be evaluated accordingly. With a temperature difference of 400 K, the maximal power output of a single TE device can be higher than 30 mW.

CHAPTER 4: Conclusion

In conclusion, the research team reports the synthesis of large-area, wafer-scale arrays of porous silicon nanowires with ultra-thin Si crystallite size of about 4 nm. Concurrent measurements of thermal conductivity, electrical conductivity, and Seebeck coefficient on the same nanowire show a *ZT* of 0.71 at 700 K, which is more than 18 times higher than bulk Si. This *ZT* value is more than two times higher than any nanostructured Si-based thermoelectrics reported in the literature at 700 K. The projects experimental data and theoretical model show that κ, σ, and S are relatively independent of temperature for the best performing SiNW, making Z independent of temperature. The model also shows that Z is relatively independent of temperature at high temperatures. Assuming this holds for temperatures greater than 700 K, a *ZT* of about 1 can be achieved at a temperature of 1000 K; however, experimental validation will require new materials for the heaters and sensors in the measurement platform, as platinum/chromium become unstable at these temperatures.

To develop practical nanowire-based thermoelectric devices, one challenge is to minimize the contact electrical resistance between the nanowire and metal electrodes for optimum current and power output. The research team successfully fabricated high-quality double-sided SiNW arrays with engineering innovations in the double-sided structure, non-agglomeration wire tip engineering, and ohmic contact formations, which enabled the team to overcome various challenges in the fabrication process and achieve uniformity in the SiNWs. The resulting high aspect ratio SiNW arrays exhibit excellent TE performance, with a maximum *ZT* of 0.24 (SiNW/SOG) at 700 K, which is among the highest reported values for SiNW arrays to date. The results highlight the potential of high aspect ratio double-sided SiNW arrays as a promising material for efficient TE energy conversion. The advanced fabrication techniques and engineering innovations demonstrated in this work could pave the way for the development of high-performance TE devices based on SiNW arrays for various energy harvesting applications. For future technology development, strategies such as chemical mechanical polishing to reduce the nanowire array top surface roughness, and subsequent rapid thermal annealing to form strong metallic bonds will be adopted.

For TE waste heat conversion to become a viable and competitive technology with other zero-carbon and waste heat conversion technologies, the levelized cost of electricity (LCOE) must be competitive. Among other things LCOE depends on the capital cost (for example, material), and lifetime the technology can survive. For example, Si-based photovoltaic (PV) has a lifetime of 25 years. Even though the efficiency of more sophisticated PV, such as fresh samples of multi-junction solar cells, is twice that of Si, Si-based PV completely dominates the market due to its low material cost, scalability, and high reliability. Although other nanostructured TE materials with higher *ZT* (2.0 or higher) have been synthesized, however, analogous to Si-based PV, Si-based TE may offer significantly lower LCOE. Therefore, the research team believes these results provide concrete material design guidelines for creating potentially highly cost-effective SiNW-based TE energy converters. The research team notes that LCOE

also depends on other factors such as integration, processing, and heat exchanger costs, however, achieving higher temperature and availability of stable and cheap TE material are very important to reduce LCOE.

GLOSSARY AND LIST OF ACRONYMS

Term	Definition
°C	degrees Celsius
°F	degrees Fahrenheit
µm	micrometer
AC	alternating current
Ag	silver
Ar	argon
Au	gold
BiTe	bismuth telluride
CHF_3	trifluoromethane
cm^{-3}	per cubic centimeter
CVD	chemical vapor deposition
DC	direct current
EBID	electron beam induced deposition
GΩ	gigaohms
H_2O_2	hydrogen peroxide
HCl	hydrochloric acid
HF	hydrofluoric acid
HNO_3	nitric acid
I-V curve	current-voltage curve
K	kelvin
LBNL	Lawrence Berkeley National Laboratory
LCOE	levelized cost of electricity
M	molarity
MΩ	megaohm
MACE	metal-assisted chemical etching
Mg2Si	magnesium silicide
mm	millimeter
mTorr	millitorr
mV	millivolt
mW	milliwatt
Ni	nickel

Term	Definition
NIL	nano imprint lithography
nm	nanometer
NW	nanowire
O_2	oxygen
PDMS	polydimethylsiloxane
Pt	platinum
PV	photovoltaic
RIE	reactive-ion-etching
s	seconds
S/m	Siemens per meter
SEM	scanning electron microscope
SF6	sulfur hexafluoride
Si	silicon
SIMS	secondary ion mass spectrometry
SiNW	silicon nanowires
SiO_2	silicon dioxide
SOD	spin-on-dopant
SOG	spin-on-glass
TE	thermoelectric
vol%	volume percent
W	watts
W/m-K	watts per meter-kelvin
wt%	weight percent
ZT	figure of merit

References

Aroutiounian, V. M. and M. Z. Ghulinyan. 2003. "Electrical conductivity mechanisms in porous silicon." *Physica Status Solidi Appl.,* 197, 462–466.

Biswas, K. et al. 2012. "High-performance bulk thermoelectrics with all-scale hierarchical architectures." *Nature*, 489, 414–418.

Borca-Tasciuc, T., A. R. Kumar, and G. Chen. 2001. "Data reduction in 3ω method for thin-film thermal conductivity determination." *Review of Scientific Instruments*, 72, 2139–2147.

Boukai, A. I. et al. 2008. "Silicon nanowires as efficient thermoelectric materials." *Nature* 451, 168–171.

Bux, S. K. et al. 2009. "Nanostructured Bulk Silicon as an Effective Thermoelectric Material." *Advanced Functional Materials*, 19, 2445–2452.

Cahill, D. G. 1990. "Thermal conductivity measurement from 30 to 750 K: The 3ω method." *Review of Scientific Instruments,* 61, 802–808.

Claudio, T. et al. 2014. "Nanocrystalline silicon: lattice dynamics and enhanced thermoelectric properties." *Physical Chemistry, Chemical Physics*, 16, 25701–25709.

Dames, C. and G. Chen. 2005. "1Ω, 2Ω, and 3Ω Methods for Measurements of Thermal Properties." *Review of Scientific Instruments*. 76, 1–14.

Díez, G. G. et al. 2020. "Enhanced thermoelectric figure of merit of individual Si nanowires with ultralow contact resistances." *Nano Energy*, 67.

Elsheikh, M. H. et al. 2014. "A review on thermoelectric renewable energy: Principle parameters that affect their performance." *Renewable and Sustainable Energy Reviews*, 30, 337–355.

Forman, C., I. K. Muritala, R. Pardemann and B. Meyer. 2016. "Estimating the global waste heat potential." *Renewable and Sustainable Energy Reviews*, 57, 1568–1579.

Geffroy, C., D. Lilley, P. S. Parez, and R. Prasher. 2021. "Techno-economic analysis of waste-heat conversion." *Joule*, 5, 3080–3096.

Heremans, J. P. et al. 2008. "Enhancement of Thermoelectric Efficiency in PbTe by Distortion of the Electronic Density of States." *Science,* 321, 554–557.

Hochbaum, A. I. et al. 2008. "Enhanced thermoelectric performance of rough silicon nanowires." *Nature*, 451, 163–167.

Jaziri, N. et al. 2020. "A comprehensive review of Thermoelectric Generators: Technologies and common applications." *Energy Reports*, 6, 264–287.

Kashiwagi, M. et al. 2019. "Scalable Multi-nanostructured Silicon for Room-Temperature Thermoelectrics." *ACS Applied Energy Materials*, 2, 7083–7091.

Kessler, V. et al. 2013. "Thermoelectric properties of nanocrystalline silicon from a scaled-up synthesis plant." *Advanced Engineering Materials*, 15, 379–385.

Kim, H. S., K. Kikuchi, T. Itoh, T. Iida, and M. Taya. 2014. "Design of segmented thermoelectric generator based on cost-effective and light-weight thermoelectric alloys." Materials Science Engineering, 185, 45–52.

Leblanc, S., S. K. Yee, M. L. Scullin, C. Dames and K. E. Goodson. 2014. "Material and manufacturing cost considerations for thermoelectrics." *Renewable and Sustainable Energy Reviews,* 32, 313–327.

Lee, J. et al. 2016. "Thermal Transport in Silicon Nanowires at High Temperature up to 700 K." *Nano Lett.*, 16, 4133–4140.

Lubner, S. D., S. Kaur, Y. Fu, V. Battaglia, and R. S. Prasher. 2020. "Identification and characterization of the dominant thermal resistance in lithium-ion batteries using operando 3-omega sensors." Journal of Applied Physics, 127, 105104.

Morata, A. et al. 2018. "Large-area and adaptable electrospun silicon-based thermoelectric nanomaterials with high energy conversion efficiencies." *Nature Communications*, 9, 1–8.

Poudel, B. et al. 2008. "High-thermoelectric performance of nanostructured bismuth antimony telluride bulk alloys." *Science*, 320, 634–8.

Schierning, G. et al. 2011. "Role of oxygen on microstructure and thermoelectric properties of silicon nanocomposites." Journal of Applied Physics, 110, 113515.

Stranz, A., J. Kähler, A. Waag, and E. Peiner. 2013. "Thermoelectric properties of high-doped silicon from room temperature to 900 K." Journal of Electronic Materials, 42, 2381–2387.

Tang, J. et al. 2010. "Holey Silicon as an Efficient Thermoelectric Material." *Nanoscale Research Letters,* 10, 4279–4283.

Tong, T. & A. Majumdar. 2006. "Reexamining the 3-omega technique for thin film thermal characterization." *Review of Scientific Instruments,* 77

Wang, X. et al. 2018. "Measuring nanowire thermal conductivity at high temperatures." *Measurement Science and Technology*, 29.

Weisse, J. M. 2013. "Fabrication and Characterization of Vertical Silicon Nanowire Arrays: A Promising Building Block for Thermoelectric Devices." Ph.D. thesis, Stanford Univ.

Weisse, J. M. et al. 2012. "Thermal conductivity in porous silicon nanowire arrays." *Nanoscale Research Letters,* 7, 554.

Yang, L. et al. 2021. "High thermoelectric figure of merit of porous Si nanowires from 300 to 700 K." *Nature Communications*, 12, 3926.

Yee, S. K., S. Leblanc, K. E. Goodson, and C. Dames. 2013. "$ per W metrics for thermoelectric power generation: Beyond ZT." *Energy and Environmental Science*, 6, 2561–2571.

Zhao, L. D. et al. 2014. "Ultralow thermal conductivity and high thermoelectric figure of merit in SnSe crystals." *Nature*, 508, 373–377.

Zhu, T. et al. 2016. "The Role of Electron–Phonon Interaction in Heavily Doped Fine-Grained Bulk Silicons as Thermoelectric Materials." *Advanced Electronic Materials*, 2, 1–6.

Project Deliverables

Deliverables for this project included:

- TAC Meeting Summary.
- SiNW Templating, Etch, and Doping Brief Report.
- Individual SiNW Thermoelectric Property Brief Report.
- Free-Standing SiNW Fill and Metallization Brief Report.
- SiNW Array Property and Characterization Brief Report.
- SiNW Array Based Device Performance Brief Report.
- SiNW Thermoelectric Device Techno-Economic Model Brief Report.
- Final Project Fact Sheet.
- Technology/Knowledge Transfer Report.

Project deliverables, including interim project reports, are available upon request at pubs@energy.ca.gov.